

MCP Code Information(2/3)

Last Updated : Jul. 2003

K	5	X	X	X	X	X	X	X	X	-	X	X	X	X	X	X	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

U : 2.7V~3.6V V : 3.0V~3.6V

Y : 2.7V~3.3V

<Only 1st Chip is NOR Flash>

E : 1.8V(1.7V~1.95V)

<Only 1st Chip is Mitsubishi NOR Flash>

N : 2.7V~3.0V

<Only 1st Chip is NAND Flash>

6 : 2.4V~2.8V

9. Flash Boot block Mode

B : Bottom Boot Block

C : Uniform Block

T : Top Boot Block

0 : NONE

10. Generation

M : 1st Generation

A : 2nd Generation

B : 3rd Generation

C : 4th Generation

11. "—"

12. Package

D : FBGA(LF)

F : FBGA

Y : TSOP1

K : TBGA(Intel Ball Out)

T : TBGA

L : TBGA(LF)

13. 1st Chip Speed

- When 1st Chip is NOR DB/BB & Mitsubishi NOR & UtRAM

1 : 100ns

2 : 120ns

3 : 85ns

6 : 60ns(except UtRAM)

7 : 70ns(except UtRAM)

8 : 80ns

9 : 90ns

- When 1st Chip is Muxed/De-Muxed NOR Flash

A : 100ns(C/F 40MHz)

B : 100ns(C/F 54MHz)

C : 90ns(C/F 40MHz)

D : 90ns(C/F 54MHz)

E : 70ns(C/F 54MHz)

F : 70ns(C/F 66MHz)

- MCP COMMON

0 : NONE

N : NO BIN(TPB)

14~15. 2nd Chip Speed

- When 2nd Chip is fCMOS SRAM & UtRAM(Muxed)

10 : 100ns

50 : 50ns

55 : 55ns

60 : 60ns

70 : 70ns

85 : 85ns

90 : 90ns

DS : Daisychain

- When 2nd Chip is TFT SRAM

85 : 85ns

- When 2nd Chip is Muxed SRAM

10 : 100ns

50 : 50ns

80 : 80ns

85 : 85ns

90 : 90ns

DS : Daisychain

- When 2nd Chip is SDRAM/DDR SDRAM

15 : 15ns@CL2

75 : 7.5ns@CL3

1H : 10ns@CL2

1L : 10ns@CL3

DS : Daisychain

- MCP COMMON

00 : NONE

16. Packing "Pcking Type Reference" (To last page)

17~18. Customer "Customer List Reference"

MCP Code Information(3/3)

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K	5	X	X	X	X	X	X	X	X	-	X	X	X	X	X	X	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

• Packing Type(16 digit)

- Common to all products, except of Mask ROM
- Divided into TAPE & REEL(In Mask ROM, divided into TRAY, AMMO Packing Separately)

Type	Packing Type	New Marking	Old Marking
Component	TAPE & REEL	T	R
	Other Packing	0(Number)	1(Number)
	Stack	S	
Component (Mask ROM)	TRAY	Y	Z
	AMMO PACKING	A	B
Module	MODULE TAPE & REEL	P	Q
	MODULE Other Packing	M	N