



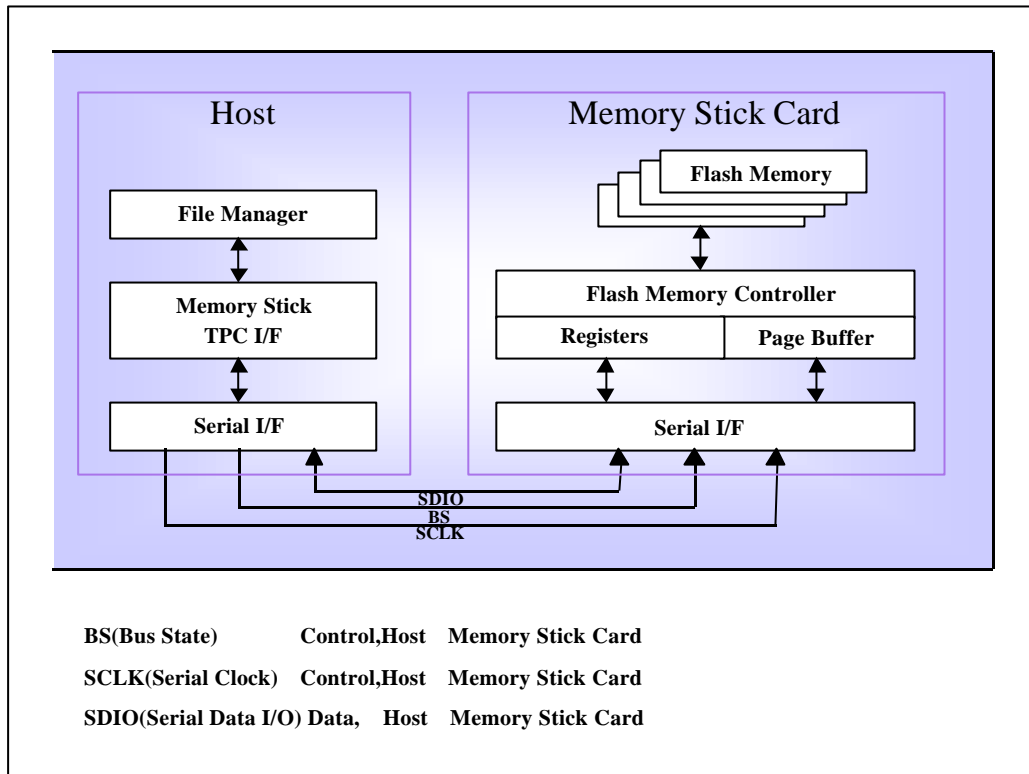
Memory Stick Information for Developers

Basic Technology on Memory Stick ▶▶ Serial I/F for Memory Stick

Basic Technology on Memory Stick

Serial I/F for Memory Stick

Block Diagram



This is Memory Stick block diagram.

Host on the left and Memory Stick on the right communicates on three signal lines.

Data is transferred on one line and other two are for regulation.

BS(Bus State) and SCLK(Serial Clock) are regulation signals from host system, and SDIO(Serial Data I/O) is two-way data signal line.

Inside Memory Stick will be explained in other pages.

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● Serial I/F for Memory Stick

Serial Interface Overview

- **Only 3 Pins**

Serial Clock

Bus State

Serial Data I/O

- **Shape Flexibility**

- **Reliability**

- **Simple Hardware Development**

Protocol is to be developed by prospective licensee

This is explanation on Memory Stick serial interface overview.

First, serial interface specifications will be explained and then command to access Memory Stick will be explained.

Memory Stick's characteristics are 1) only 3 signal lines for connection; 2) shape is flexible; 3) height reliability; 4) simple hardware development.

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Protocol Overview

- **Four Bus State: SDIO Data acknowledgement**

BS0: Idling

BS1: TPC(Transfer Protocol Command)

BS2,3: Data/Hand-shake

- **TPC and Flash Command**

- **CRC16 Data Error Detection**

- **Handshake**

- **Interrupt Signal**

Serial protocol overview.

Serial interface protocol consists of 4 bus states, and bus state is used to serial data type.

BS0 is idling, BS1 is host transferring TPC, BS2 and BS3 are handshake and data transfer states which depends on read/write operations.

TPC and flash commands are defined.

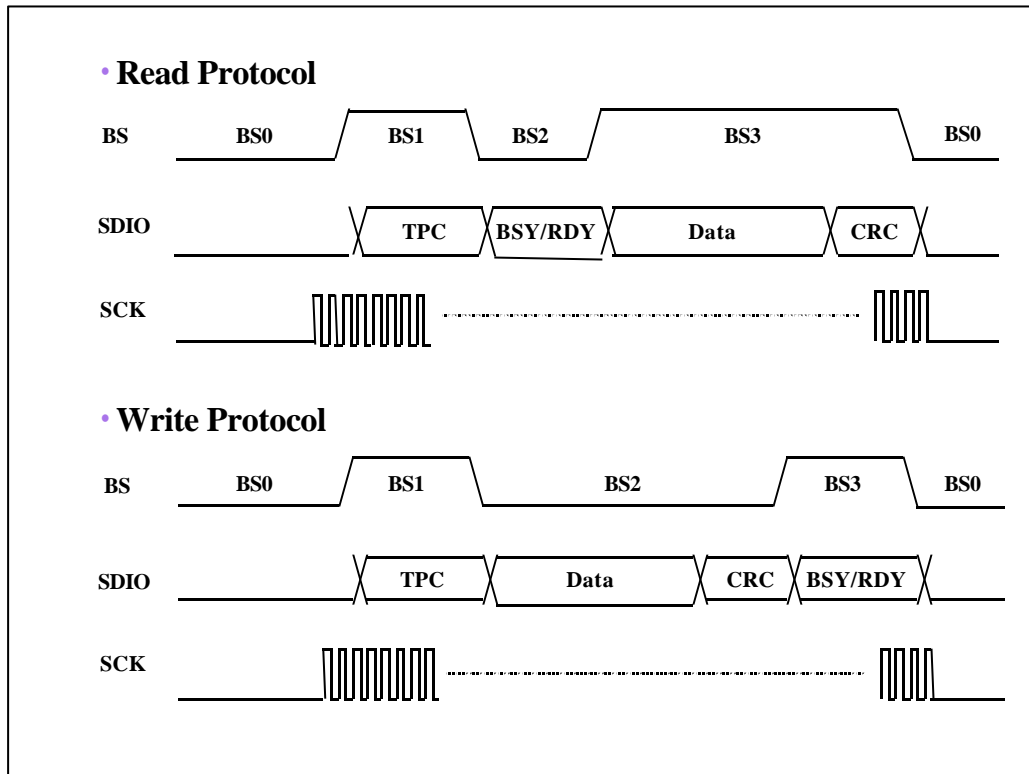
Data error is detected by CRC16. Handshake occurs between Memory Stick and host.

Host receives interruption signal from Memory Stick and processed.

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Serial IF Signal Wave Form- 1:Read•Write



Serial interface read/write running chart.

Serial interface signal wave form consists of protocols on three signal lines. As SDIO is for data, signal runs to both directions. BS stands for bus state, and BS levels show data flow directions and data type on SDIO.

There are four bus states.

First bus state upon read is BS0: IDLE. Signal is always low.

Second is BS1. TPC command will be sent to Memory Stick.

Third is BS2, which is Handshake. Memory Stick returns busy signal, and when it can output data, returns ready signal. Fourth is BS3, when data and CRC is read from Memory Stick.

Upon write, as shown, data and CRC is processed during BS2 and busy/ready signal during BS3.

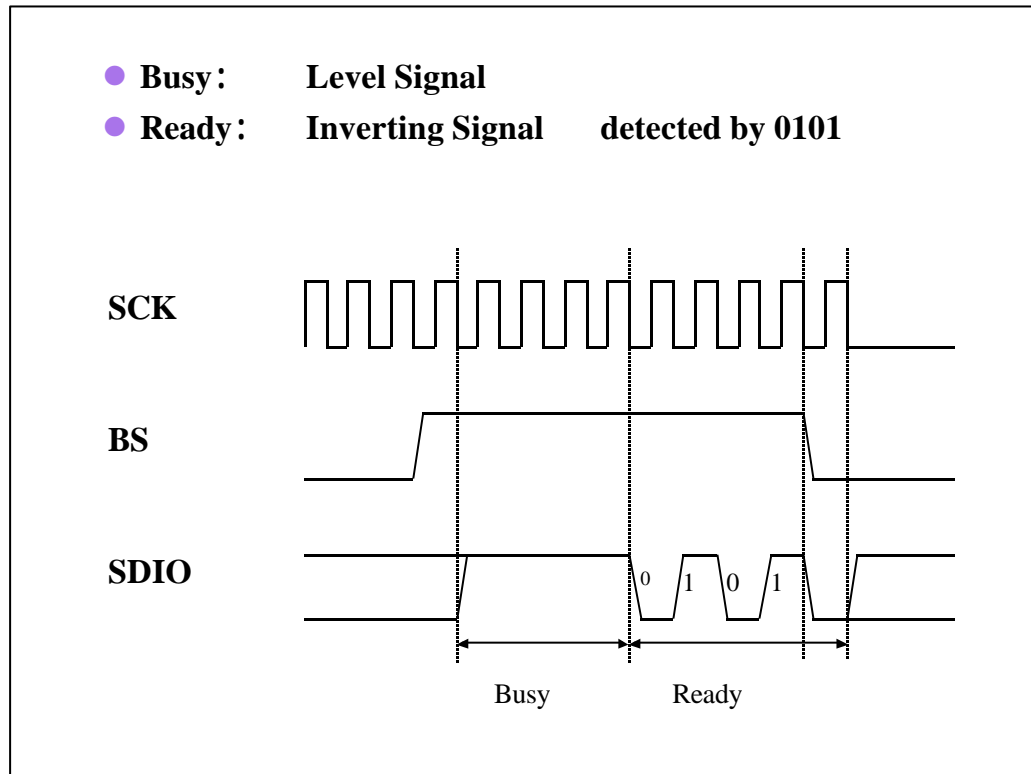
Bus state sequence are different between read and write operations.

SCLK means clock.

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Serial IF Signal Wave Form- 2: Hand-shake



The table shows handshake state.

BUSY means TPC which Memory Stick received is under process.

Signal is high level.

RDY means TPC process is ended without problem.

Signal is inverting.

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Serial IF Signal Wave Form- 3:Interrupt(INT)

- **SDIO level detect during BS0**
- **Inform command process completion from Memory Stick to Host**

Interrupt occurrence factor is reflected to INT Register
INT Register

*After execution of Flash Control Command, output during BS0 period.
 (Read, Write, Erase command for flash memory)*

This is explanation on interrupt signal(INT).

Interrupt signal is sent from Memory Stick.

Interrupt signal is detected by monitoring SDIO level during BS0.

Interrupt means that memory control command is processed without problem from Memory Stick to host.

Interrupt occurrence factor is reflected to INT register.

Flash Memory Controller process takes as long as several hundred μ as data is written actually. Process end needs to be informed to Host other than protocol ends.

This is done by driving SDIO to High during BS0.

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TPC Code

TPC = 4Bit(Original)+4Bit(Reverse)

Code	Name	Data Size	Description
B'0010	READ_PAGE_DATA	512Byte	Read Page Buffer
B'0100	READ_REG	1 ~ 31Byte	Read Status & Extra Data Registers
B'0111	GET_INT	1Byte	Read INT Register
B'1101	WRITE_PAGE_DATA	512Byte	Write Page Buffer
B'1011	WRITE_REG	1 ~ 31Byte	Write Parameter & Extra Data Registers
B'1000	SET_R/W_REG_ADRS	4Byte	Set Reg Address for READ/WRITE_REG
B'1110	SET_CMD	1Byte	Set Flash Control Command

A list of TPC which is equivalent to commands transferred by Protocol.

To access inside Memory Stick, there are three operations;

Read/Write to Page Buffer

Read/Write of Register

Command Transfer to Flash Memory Controller

Interrupt occurrence factor detection, there is GET INT command.

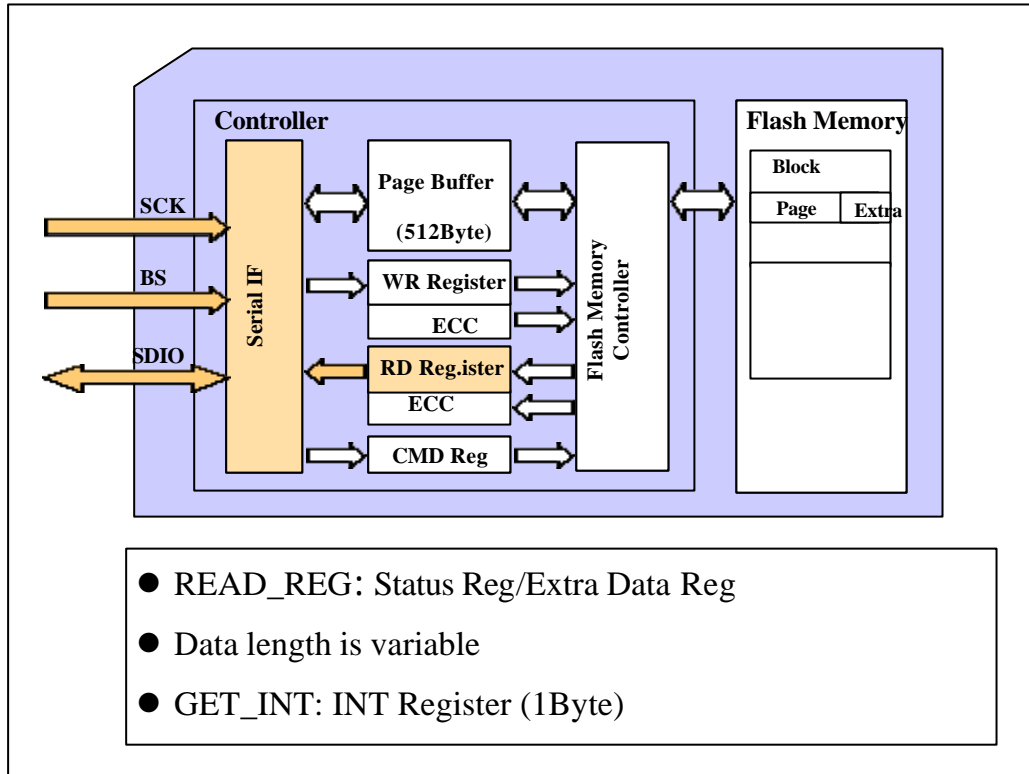
SET CMD is flash control command defined in the byte following the above TPC.

To send command to flash memory, this command is executed.

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TPC - : READ_REG/GET_INT



This shows read register.

Read register reads out register data to host.

Status Reg/Extra Data Reg are read.

Data length is variable.

Host reads the first 1 byte of GET_INT.

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Register Map 1: Read

Read	
H'01	INT Register
H'02	Status0 Register
H'03	Status1 Register
H'15	Page Address
H'16	Overwrite Flag
H'17	Management Flag
H'19	Logical Address 1
H'1	Logical Address 0
A	Reserved Area 4
H'1B	Reserved Area 3
H'1	Reserved Area 3
C	Reserved Area 2
H'1D	Reserved Area 1
H'1E	Reserved Area 0

- Status Registers**
 - INT Register INT(BS0) Details
 - Status0 Reg Busy, Sleep, Write Protect, Page Buf Status
 - Status1 Reg FlashError Details
- Extra Area Data Read Registers**
 - OverwriteFlag
 - Block, Page Allocation Info
 - Management Flag
 - MS Format Defined
 - Logical Address 1 ~ 0
 - Reserved Area 4 ~ 0

This is register list. There are three sections;

Status including INT Register

Command Parameters

Control information called Extra Area in each Page

Busy, Sleep, Write Protect, Page Buffer Status will be written in status 0 register.

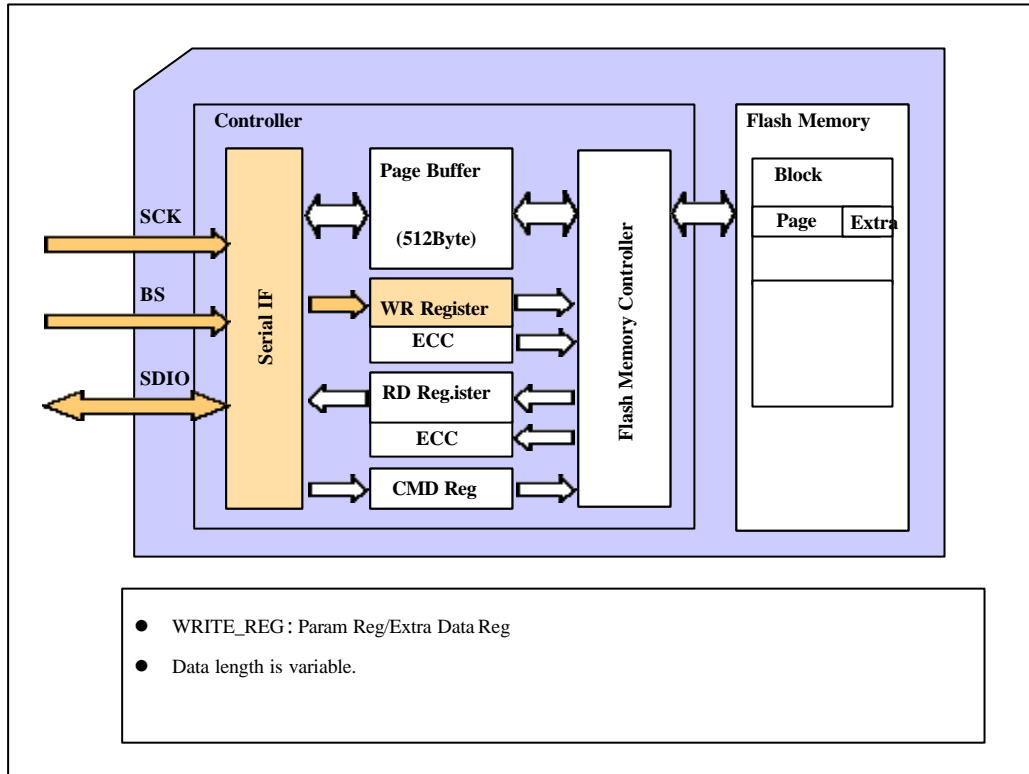
Status 1 register contains information on errors occurred in flash memory.

Extra Area Data Read Register contains information of flash memory extra area. Overwrite flag and logical address are examples.

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TPC - 2:WRITE_REG



This shows write register.

Write register specifies parameter such as flash memory block address or set data for flash memory extra area.

Write register is Param Reg and Extra Data Reg. Data length is variable.

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Register Map 2: Write

Write	
H'10	System Parameter
H'11	Block Address 2
H'12	Block Address 1
H'13	Block Address 0
H'14	Command Parameter
H'15	Page Address
H'16	Overwrite Flag
H'17	Management Flag
H'18	Logical Address 1
H'19	Logical Address 0
H'1A	Reserved Area 4
H'1B	Reserved Area 3
H'1C	Reserved Area 2
H'1D	Reserved Area 1
H'1E	Reserved Area 0

- Parameter Registers**
 - Block Address 2 ~ 0
 - Command Param
 - Data/ExtraArea Selection
 - OverwriteMode
 - ContinuousMode
 - Page Address
- Extra Area Data Write Registers**
 - Overwrite Flag
 - Management Flag
 - Logical Address 1 ~ 0
 - Reserved Area 4 ~ 0

This is list of write registers.

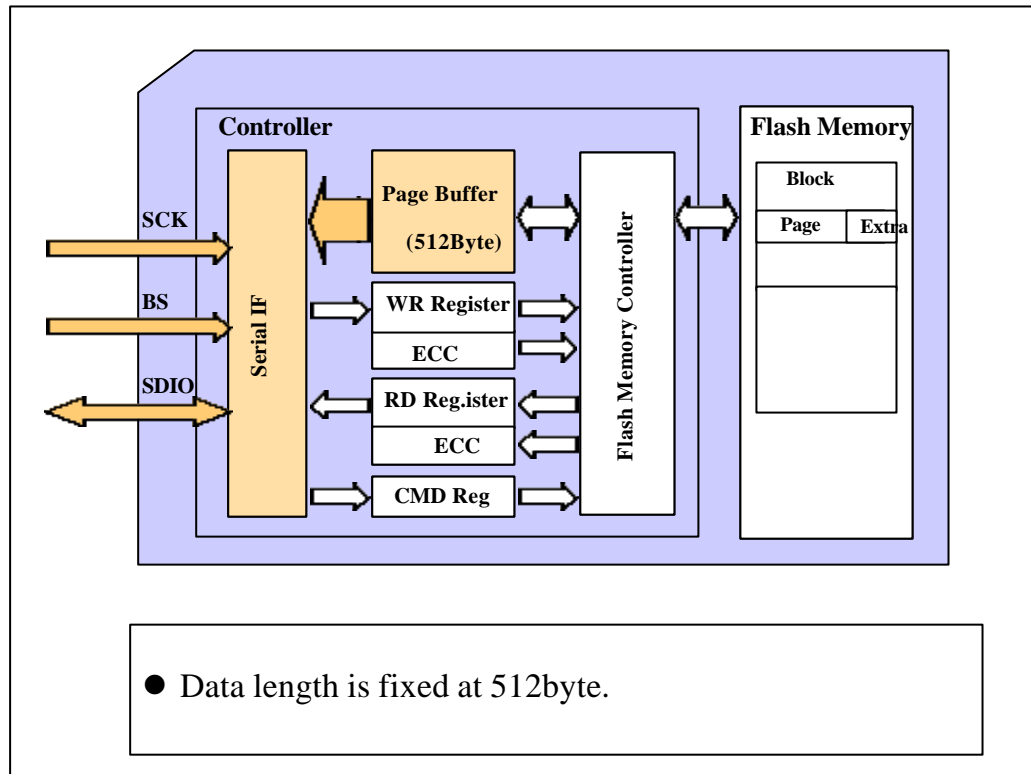
Parameter registers consist of block address, command parameter, page address, etc.

Extra area data write registers contain data to be written in the extra area.

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TPC - 3 : READ_PAGE_BUF



This shows read page buffer.

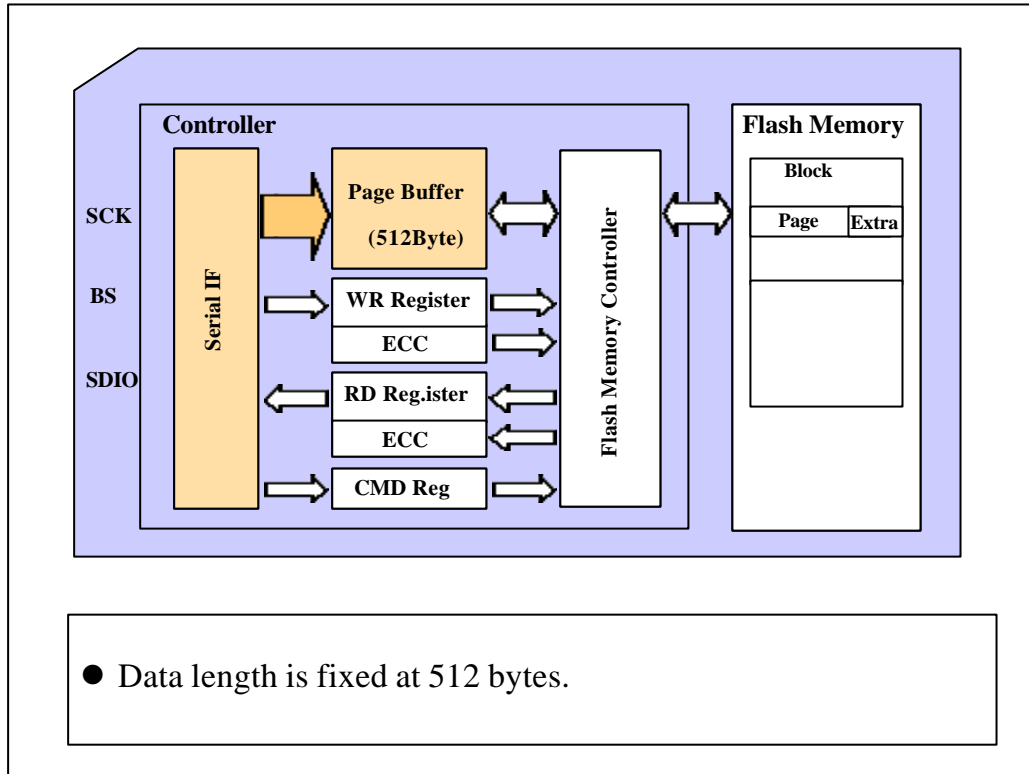
Page buffer data is read by host.

Data length is fixed at 512 bytes.

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TPC - 4 : WRITE_PAGE_BUF



This shows write page buffer.

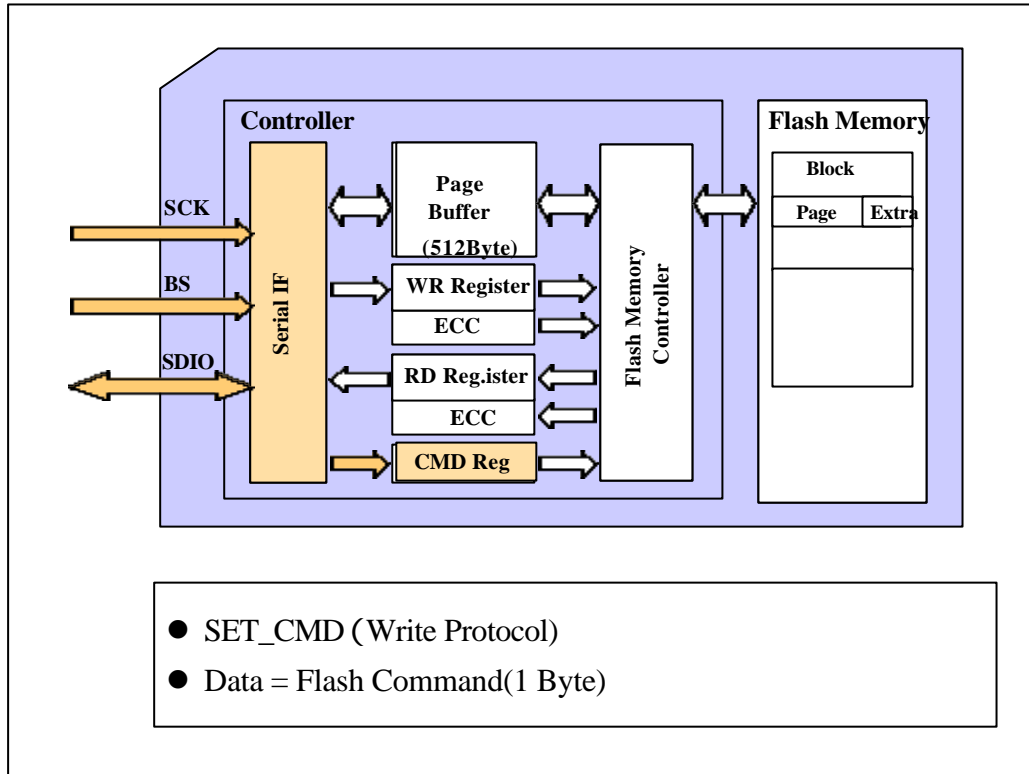
The command is used when host write in the page buffer.

Data length is fixed at 512 Bytes.

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TPC - 5 : SET_CMD



This shows set command.

Set command is used when host write flash memory command in CMD register. It is write protocol. Data is one-byte flash command.

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Flash Command

SET_CMD: Write Protocol

Code	Name	Description
H'AA	BLOCK_READ	Read to Page Buf from Flash Memory
H'55	BLOCK_WRITE	Write from Page Buf to Flash Memory
H'33	BLOCK_END	Stop Continuous Read/Write
H'99	BLOCK_ERASE	Erase Block
H'CC	FLASH_STOP	Reset Flash Memory Busy
H'5A	SLEEP	Sleep Flash Controller
H'C3	CLEAR_BUF	Clear Page Buf
H'3C	RESET	Reset Flash Controller, Clear Register

This is a list of flash memory controller command transferred by SET_CMD TPC.

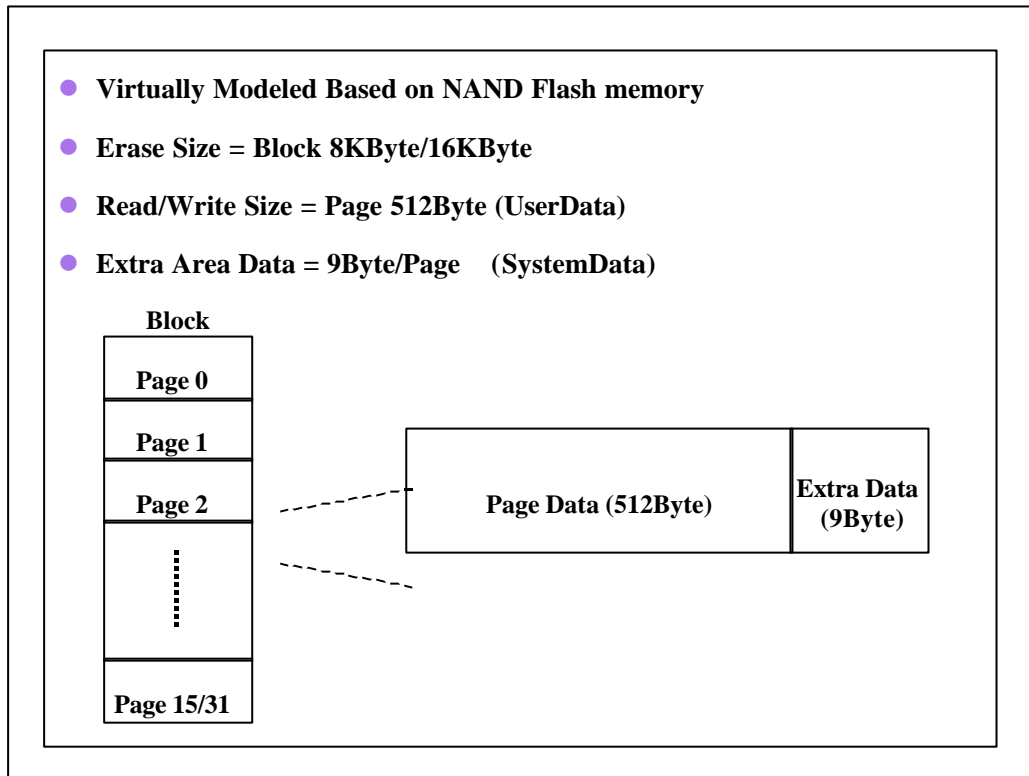
There are block read, block write, block erase, stop and page buffer clear.

These are all about serial interface overview.

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Flash Memory Model



Flash Memory Model.

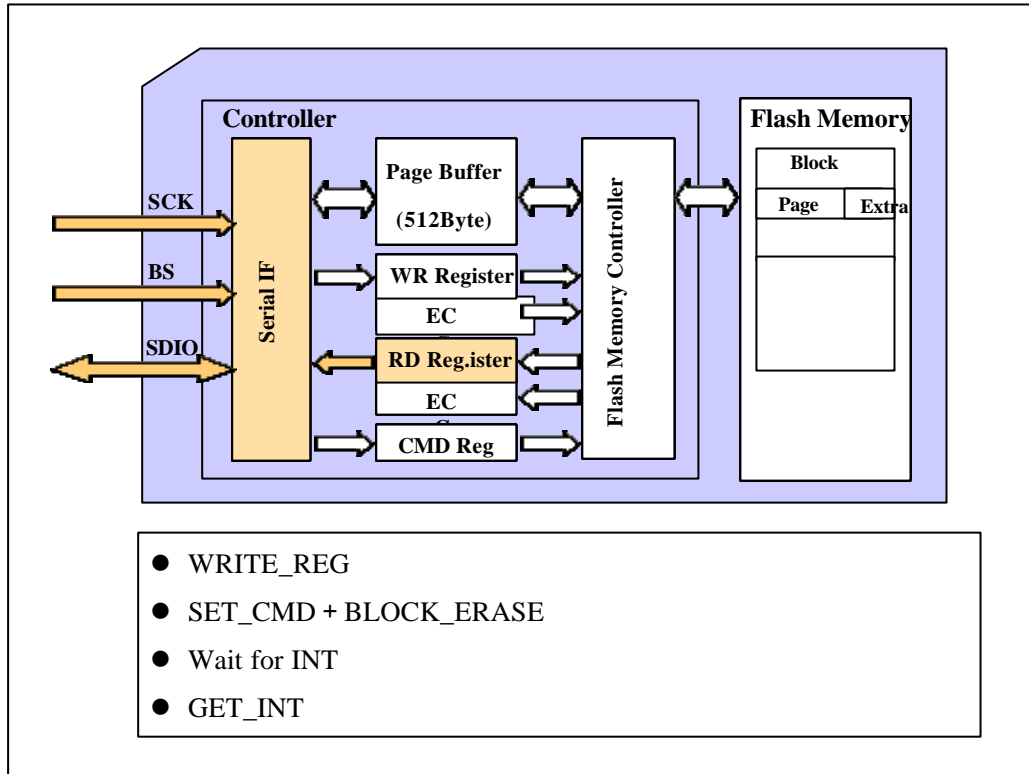
Flash memory in Memory Stick is virtually modeled to host so that not only NAND but also various types of flash memory chips can be used for Memory Stick. Each type of flash memory chip requires corresponding controller in Memory Stick.

Specifications of memory model is shown in the chart. Basically NAND flash memory is to be used and erase unit is block, which is 8 or 16 K Byte. Read/write unit is page, which is 512 K Byte.

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CMD - 1 : Erase Block



This shows erase block and the process to erase a part of data in flash memory.

First, parameter such as flash memory address to erase is written in the write register.

Second, "Set CMD-Block ERASE" command is set in command register.

Then erase starts and host waits for INT.

Once erase is completed, INT signal is released.

Host send "GetINT" command, end signal is read out from Read Reg.

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INT Register

• INT Register

D7	D6	D5	D4	D3	D2	D1	D0
CED	ERR	BREQ	-	-	-	-	CMDNK

CED	ERR	BREQ	CMDNK	Description
1	0	X	0	Completed Successfully
1	1	X	0	Completed with Flash Error
X	0	1	0	Data Request (Continuous Mode)
X	1	1	0	Data Request with Correctable Read Error (Continuous Mode)
X	X	X	1	Command Nack

This is data in INT register.

When flash memory controller executes a process by SET_CMD TPC, the result will be indicated.

CED : command end

ERR : read, write, erase error

BREQ : write request to PageBuffer

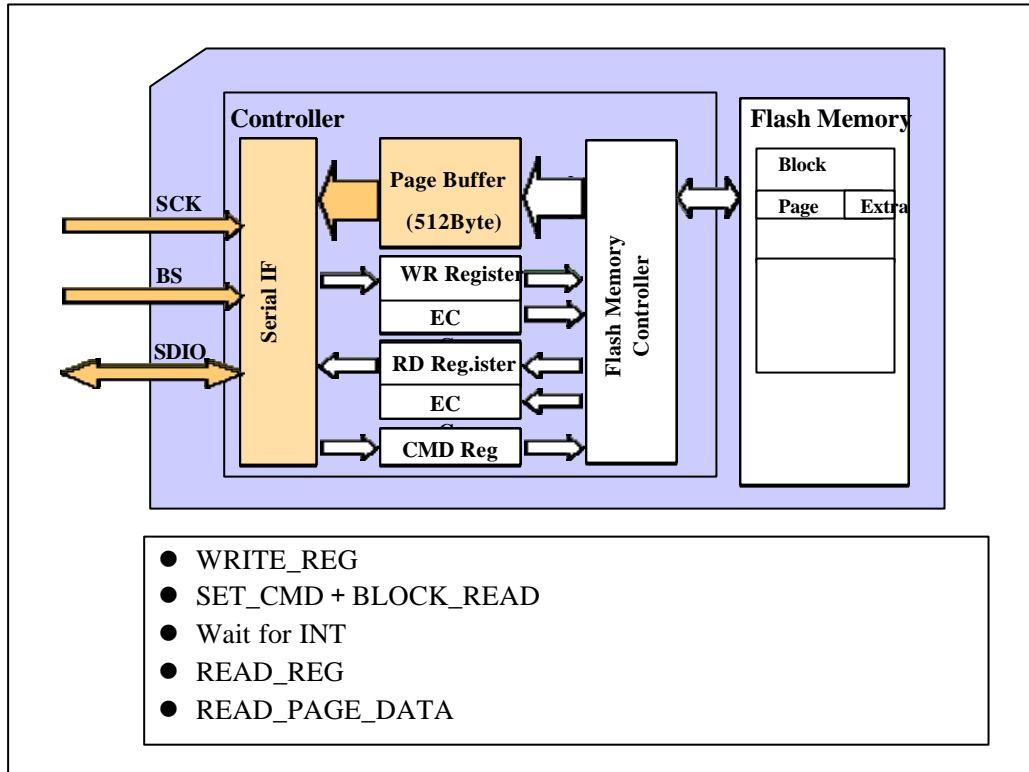
CMDNK : no-executable command by parameter error, etc

When INT register is read, INT signal is disengaged during BS0 and return to Low.

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CMD - 2 : Read Page



Read page process.

First, parameter to flash memory is specified in write register.

Second, "block read" set command is issued. Then read process is executed to flash memory,

And INT signal is waited.

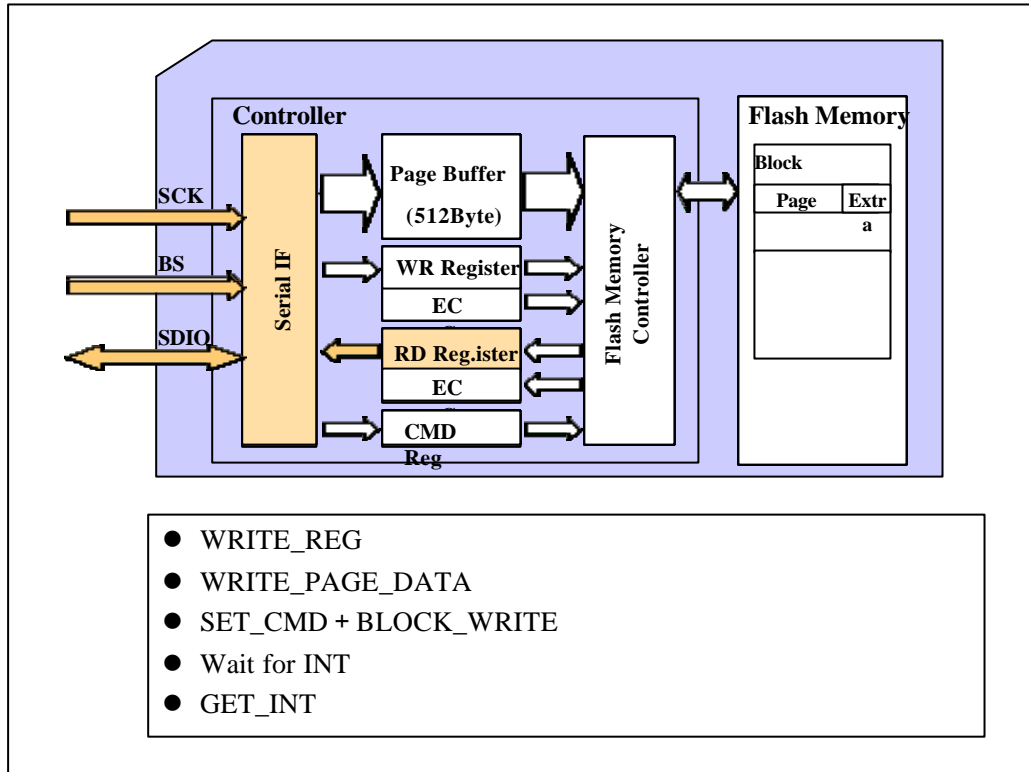
When data is read out into page buffer, INT is issued. At that point, read register reads out status and extra area data.

Lastly, Read_Page_Data is executed and host reads actual data.

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CMD - 3 : Write Page



WritePage process.

First, parameter information is set in write register.

Then the write data is sent to page buffer through the WRITE-PAGE-DATA.

Next “block write” command is issued.

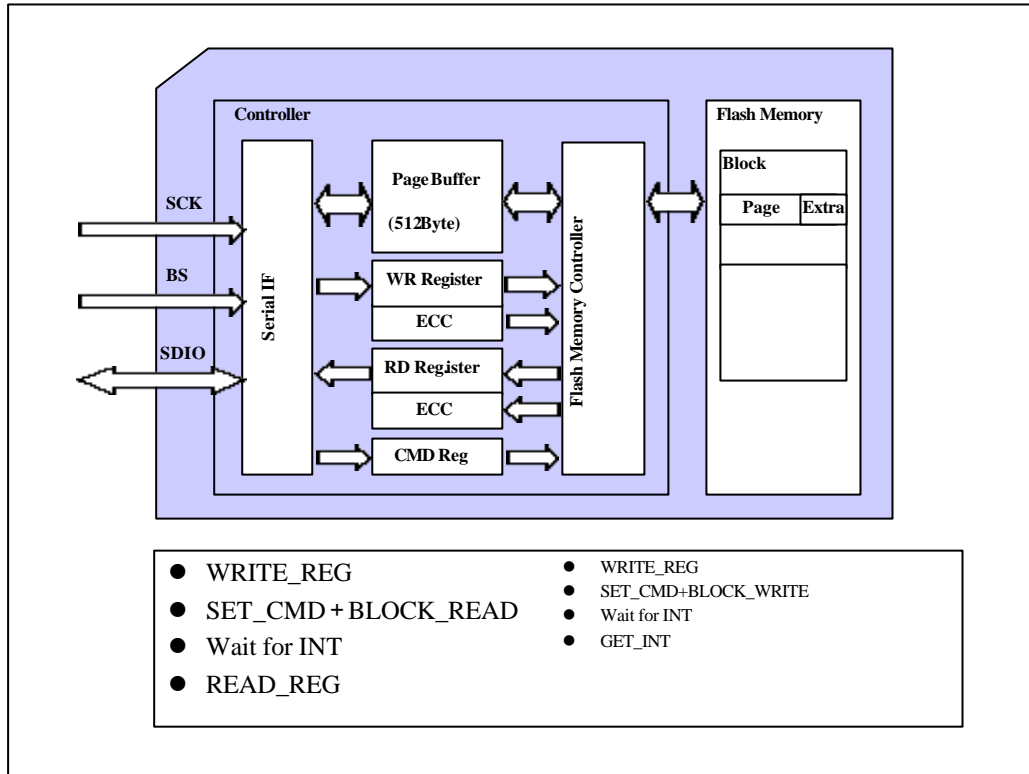
Then write process to flash memory starts, and INT signal is waited.

Host reads INT signal from read register by “Get INT” command.

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CMD - 4 : Copy Page



Copy page process, which copies data of a pager to another page.

Fist data is read out to page buffer, new address is set in write register, and write command is issued.