Memory Stick Information for Developers

Memory Stick ▶▶ Serial Interface

5. Serial Interface

5.1. System Configuration

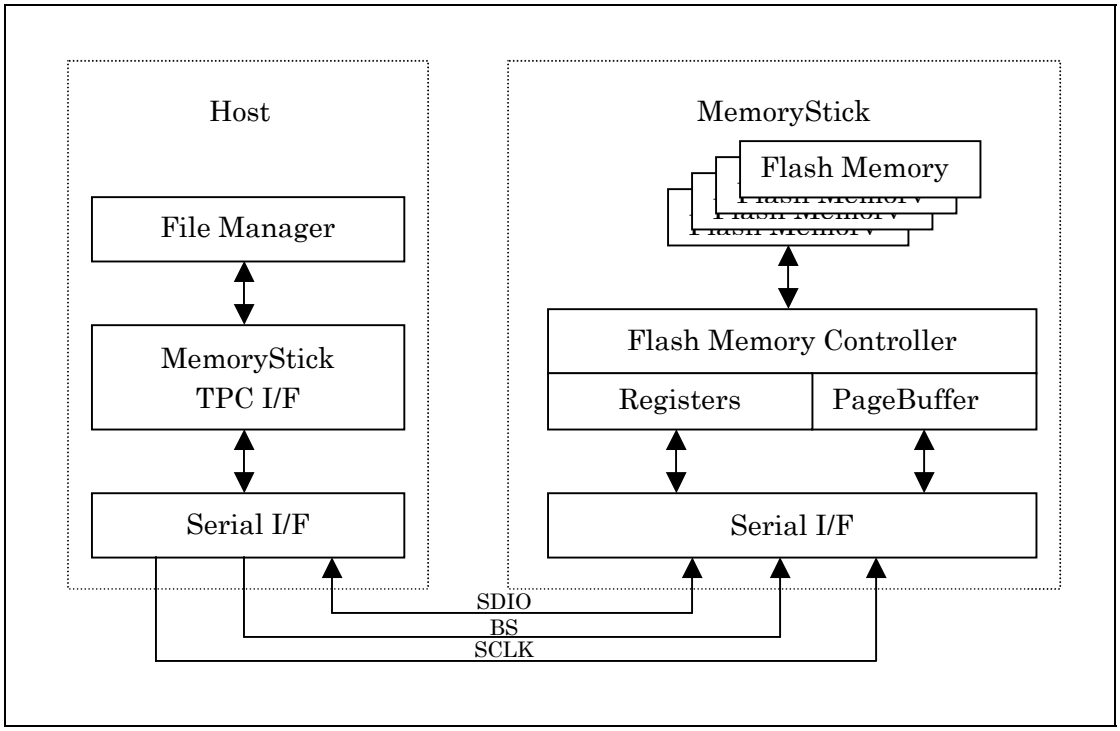


Fig. 5.1.1 System Construction

Memory Stick consists of Serial I/F, Registers, PageBuffer, Flash Memory Controller and Flash Memory.

Serial I/F regulates the protocol to transfer optional data on three signal lines of SCLK (Serial Clock), BS (Bus State) and SDIO (Serial Data In/Out).

Host accesses to Register group and PageBuffer on Memory Stick using TPC (Transfer Protocol Command).

Flash Memory Controller in Memory Stick transfers data between PageBuffer and Flash Memory based on parameter values set by Register group, then reads, writes and erases data.

The Flash Memory is capable of structuring its unique Memory Model in a 'virtual' sense through mediation of Flash Memory Controller regardless of the memory type. (See Table 5.1.1)

Table 5.1.1 Memory Model

Item	Specifications	
Initial value of data	0xFF (Value just after erase)	
Block size (Erase size)	8K bytes, 16K bytes 2 size types are not allowed to exist on same Card.	
Page size (Read/write size)	One page consists of two areas : DataArea and ExtraDataArea. See Note 1) for restrictions on sequence of using pages in a Block. ECC is used to ensure data reliability.Note 3)	
	Data area	512 bytes
	ExtraDataArea	OverwriteArea : 1 byteNote 2) NonOverwriteArea : 8 bytes
Erase timeNote 4)	Less than 100ms (Includes operating time of Flash Memory Controller)	
Write timeNote 4)	Less than 10ms (Includes operating time of Flash Memory Controller)	
Read timeNote 4)	Less than 5ms (Includes operating time of Flash Memory Controller)	
Stop timeNote 4)	Less than 5ms (Includes operating time of Flash Memory Controller)	
Guaranteed number of overwrites to ExtraDataArea	2 times or more	

Note 1) Restrictions on sequence of using a page in a Block.
Once writing to Block b starts from page p1(p1>0), writing to Block b after that can be made only to pages p>p1. If writing is made to page p<p1, all data written in every page in Block b is not to be guaranteed.

Note 2) OverwriteArea
Only "1→0" overwrite is allowed for each bit. Overwriting of a bit, which is already 0, is done with a data masked with 1.
e.g.: Overwrite D7 of 0xF0 to 0;
Masked data = 0x7F
Result 0xF0 →0x70

Note 3) ECC
The optimal ECC for Flash Memory shall be used.
e.g.: NAND flash;
1-bit error correction, 2-bit error detection

Note 4) Definition of Erase, Write, Read and Stop Time:
Maximum time from transferring the command using SET_CMD TPC till generating INT.

5.2. Serial I/F Overview

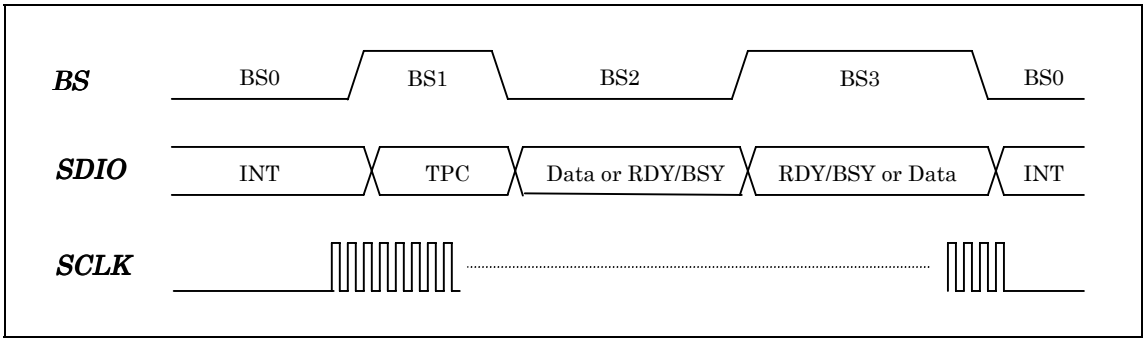


Fig. 5.2.1 Serial I/F Signals

Three signal lines connect host and Memory Stick. Communication is always started from Host.

Table 5.2.1 Serial I/F Signal Specifications

Signal	Host side	Description
BS (BusState)	Output	Indicates Bus State(0~3) on SDIO and its timing of starting transfer.
SCLK (SerialCLocK)	Output	Signal on BS and SDIO is output at trailing edge and input (latched) at leading edge. It is always output except for BS0 period.
SDIO (Serial Data In/Out)	Input/ Output	Serial data bus. The direction of the data and the data itself will change at each Bus State. Data is 8bit, MSB First.

BS signal classifies data on SDIO into four states according to the attribute and transfer direction; one state (BS0) with no packet communication going on, and three (BS1, 2, and 3) states with packet communication being executed, and controls the timing of data output. BS1 through BS 3 are dealt as one packet, and one communication is always completed within one packet. (In Four State Access Mode.)

Table 5.2.2 Bus States in Four State Access Mode

State	BS	Description	
BS0	Low	INT Transfer State A state in which packet communication is not active, and used as a transmission line for INT signals (interruption).	
BS1	High	TPC State Packet starts, and transfers TPC (Transfer Protocol Command) from Host to Memory Stick.	
BS2	Low	For read protocol	For write protocol
		Handshake State : Waiting for RDY signal.	Data Transfer State : Transferring data to Memory Stick.
BS3	High	For read protocol	For write protocol
		Data Transfer State : Reading data from Memory Stick.	Handshake State : Waiting for RDY signal.

Memory Stick usually operates in Four State Access Mode from BS0 through BS3. However, if an error occurs during packet communication, the mode is shifted to Two State Access Mode in which states BS0 and BS1 are automatically repeated to avoid bus collision on SDIO. (See Section 5.4.)

5.3. Protocol

Bus State sequences of write packet which transfer data from Host to Memory Stick differ from those of read packet which transfer data from Memory Stick to Host.

5.3.1. Write Packet

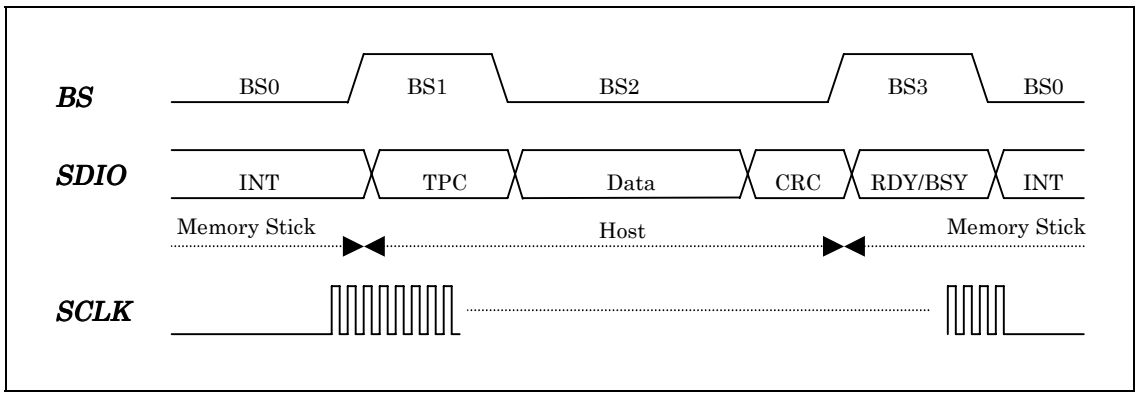


Fig. 5.3.1 Write Packet

Table 5.3.1 Write Packet

Bus State	Direction	Description
BS1 (TPC)	Host → Memory Stick	Transfers Write TPC.
BS2 (Data)	Host → Memory Stick	Transfers Data + CRC to SDIO from Host.
BS3 (Handshake)	Memory Stick → Host	During BSY output (High/Low signal) on SDIO, Memory Stick decides whether packet can be terminated normally or not, and reflects the result to the corresponding register, then outputs RDY(a signal inverting at every 1SCLK) on SDIO.
BS0 (INT)	Memory Stick → Host	If some interruption factors occur as a result of Memory Stick inner operation, INT (High signal) is output on SDIO. During BS0 period, SDIO signal line is used as INT signal line which does not synchronize with SCLK.

5.3.2. Read Packet

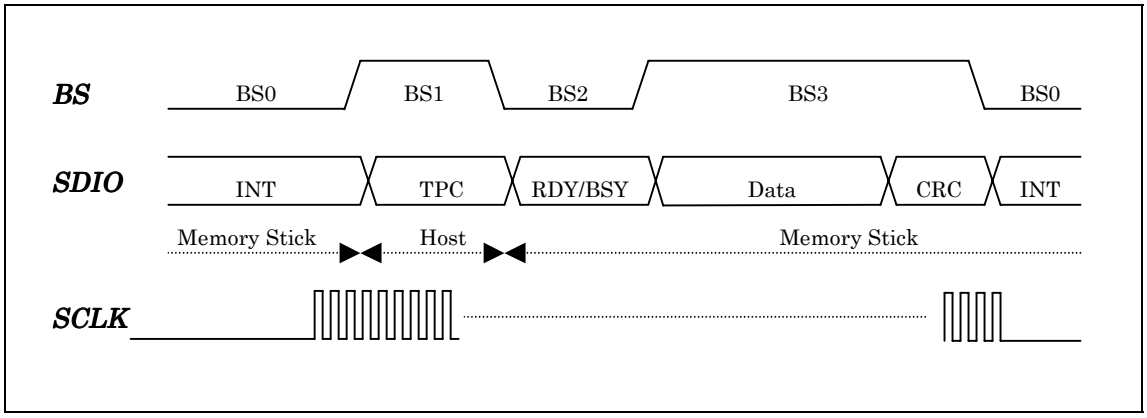


Fig. 5.3.2. Read Packet

Table 5.3.2 Read Packet

Bus State	Direction	Description
BS1(TPC)	Host → Memory Stick	Transfers Read TPC.
BS2 (Handshake)	Memory Stick → Host	Memory Stick outputs BSY(High/Low signal) on SDIO till reading data is ready to transfer. When ready, it outputs RDY (inverting signal at every 1SCLK).
BS3(Data)	Memory Stick → Host	Data + CRC are output on SDIO from Memory Stick.
BS0(INT)	Memory Stick → Host	If some interruption factors occur as a result of Memory Stick inner operation, INT (High) signal is output on SDIO. During BS0 period, SDIO signal line is used as INT signal line which does not synchronize with SCLK.

5.4. Protocol Error

5.4.1. Overview

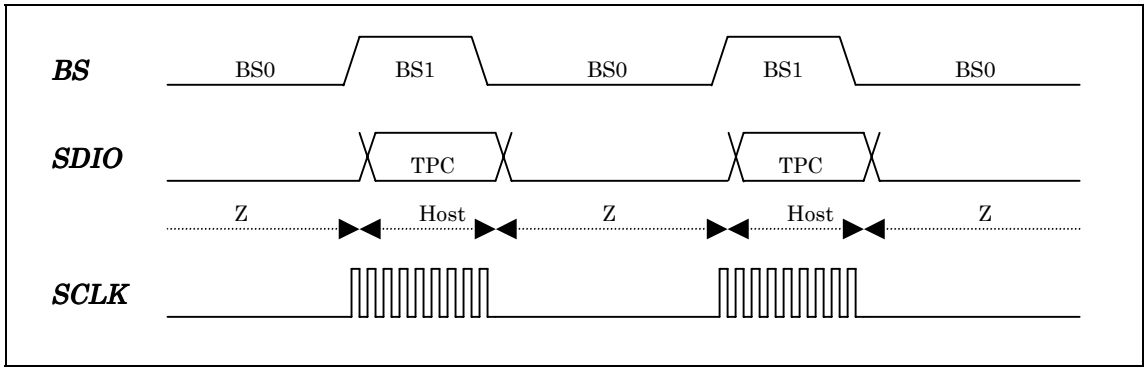


Fig. 5.4.1 Two State Access Mode

Since High and Low BS signals express Bus States respectively, bus collision occurs if a difference in Bus State between Host and Memory Stick arises for some cause.

To avoid this, Memory Stick shifts to Two State Access Mode automatically when an error occurs in packet.

In Two State Access Mode, operation is performed with recognition that BS=L is BS0 and BS=H is BS1.

Table 5.4.1 Bus State in Two State Access Mode

BusState	Direction	Description
BS0	—	Under normal condition, it is regarded as high impedance state, regardless of INT signal output period. There is no output even if INT signal is active.
BS1(TPC)	Host → Memory Stick	Memory Stick accepts TPC.

When Memory Stick shifts to Two State Access Mode, timeout occurs at Handshake State of packet on Host, and the failure of communicating packet is detected.

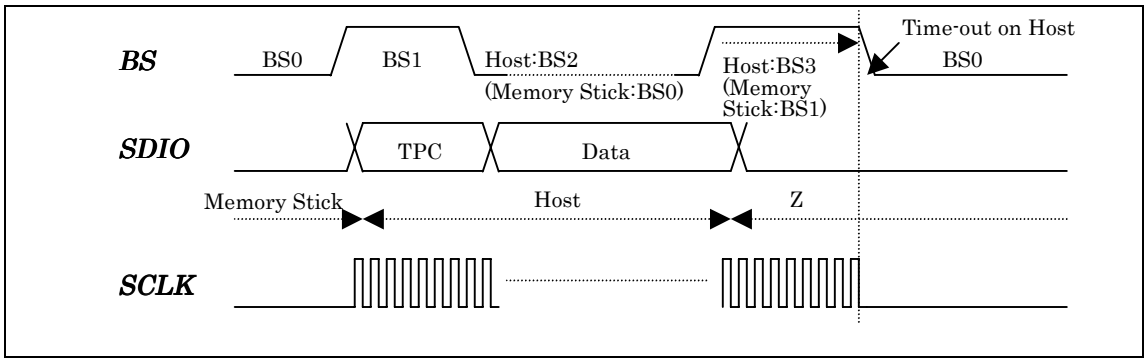
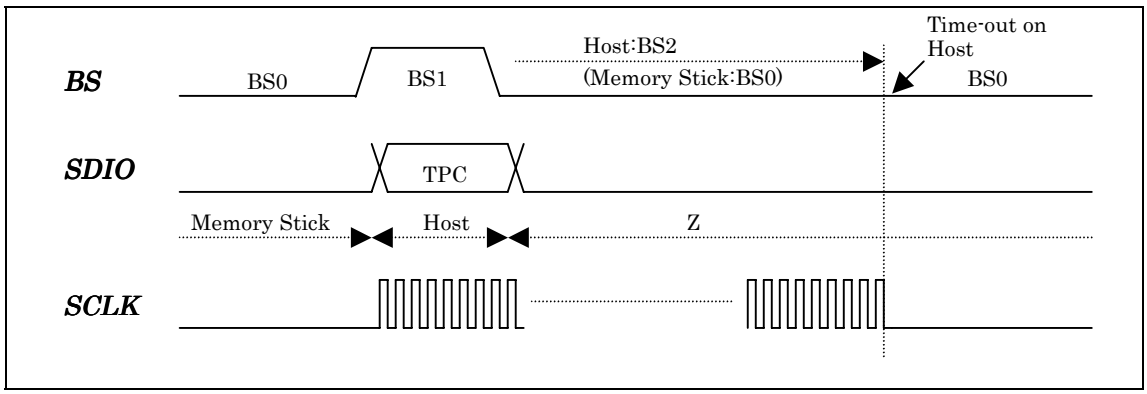


Fig. 5.4.2 Write Packet Timeout



Note) If timeout occurs in BS2 of read packet, Bus State will not shift to BS3.

Fig. 5.4.3 Read Packet Timeout

5.4.2. Two State Access Mode Factor

5.4.2.1. TPC Code Error

- 4 Bit Error Check Code Error
- Undefined TPC
- Unacceptable TPC (TPC is received but Memory Stick is not capable of executing it due to internal status.)
- Short TPC State (When BS1 is under 8SCLK.)

5.4.2.2. Data Error

- Write packet CRC Error (CRC Error occurred in the data transferred from Host.)
- Short Data State (Not all data are accepted because data state of BS is shorter than the setting on Memory Stick.)

5.4.2.3. Handshake Error

- Short Handshake State (BS is switched before the output of RDY, though Memory Stick is operating normally.)

5.4.2.4. Power Supply ON

5.4.3. Return to Four State Access Mode

If any error factor described above does not occur in BS1, the mode will shift to BS2, BS3 and enter Four State Access Mode. When an error described above occurs, it will return to Two State Access Mode again.

5.5. Signal Timing

5.5.1. Timing

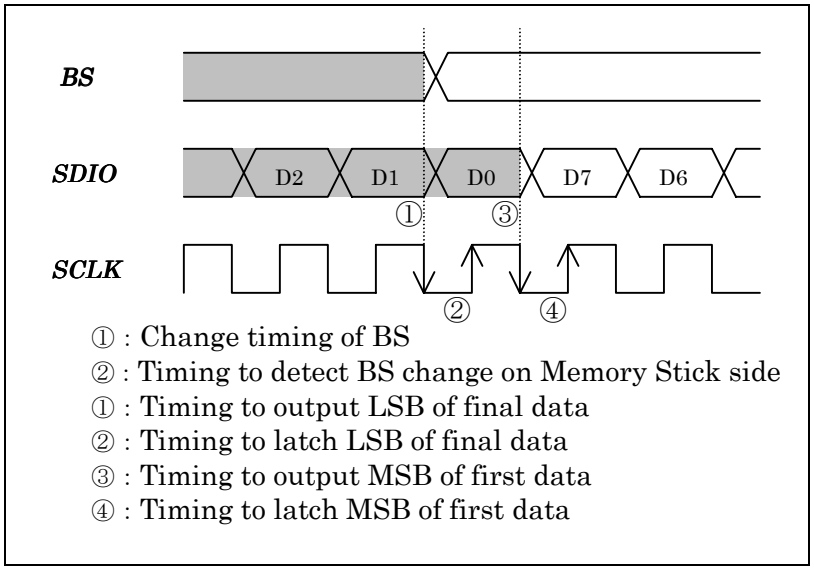


Fig. 5.5.1 Signal Timing

- Timing of SCLK, SDIO and BS
  Sender outputs SDIO signal at SCLK fall (output side), and latches it at SCLK rise (input side).
- BS signal is output synchronizing with SCLK fall.
- Relation between BS change and data
  When BS changes to shift to the next state, and Bus State is not extended, new BS is output synchronizing with the output timing of final data LSB on SDIO in the previous state.
- TPC, data and CRC are MSB first.

5.5.2. Bus State Extension

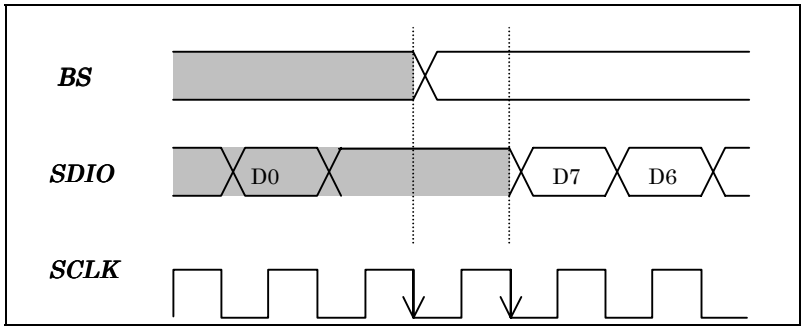


Fig. 5.5.2 Bus State Extension

If it is difficult to switch BS signal in the same timing as the final data, in TPC State and Data State, it is possible to continue that Bus State without switching the BS signal even after the final data transfer.

However, in Data State, High must be output on SDIO during the period when Bus State is continued without switching after the transfer of the last bit. In TPC State, signals on SDIO in this period are not prescribed.

5.5.3. Data Transfer Extension

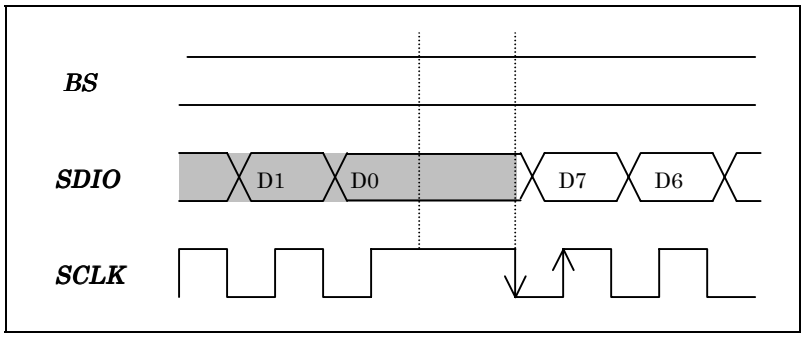


Fig. 5.5.3 SCLK Extension for Data Wait

When data transferred from Host cannot be output to catch the next fall of SCLK for some cause, or data transferred from Memory Stick to Host cannot be received from the rise of next SCLK because the buffer is full on Host, the next data transfer can be delayed by keeping SCLK high.

5.6. Bus State

5.6.1. TPC State (BS1)

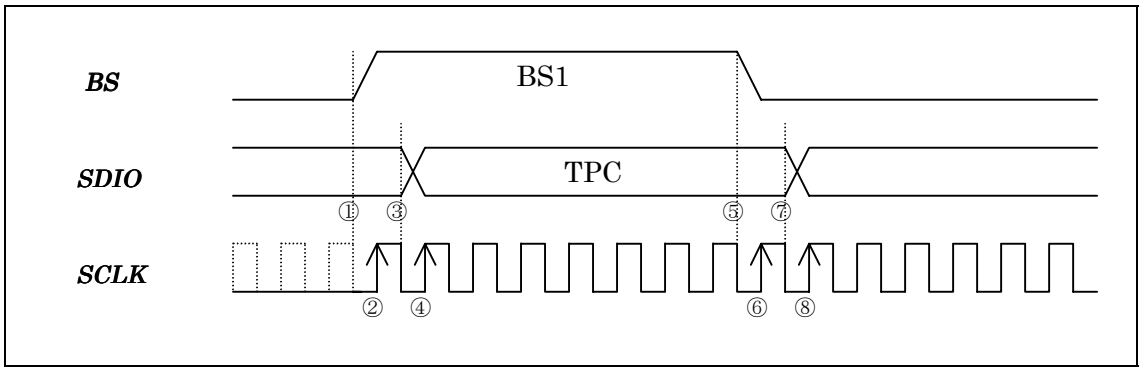


Fig. 5.6.1 TPC State (BS1)

Table 5.6.1 TPC State (BS1)

Host	BS=High is output at timing ①, and SCLK supply is started before timing ②. Output is started from MSB of TPC to SDIO at timing ③. LSB of TPC is output at timing ⑤ and BS=low is switched simultaneously, and output of BS2 is started from timing ⑦.
Memory Stick	BS=High is detected at timing ②, and MSB of TPC is received at timing ④. LSB is received at timing ⑥ and at the same time BS=Low is detected. BS2 output is started from the timing ⑦. As described before, the next state becomes BS0 if an error occurs, and in normal state, operation that TPC commands is started.

TPC State receives initial 8 SCLK data as TPC, and ignores the rest.

5.6.2. Data Transfer State (BS2 : In Write Packet)

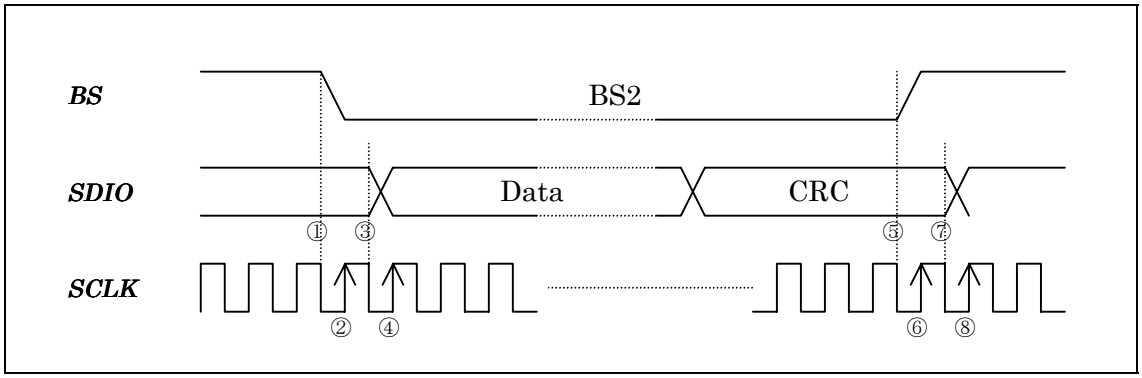


Fig. 5.6.2 Data Transfer State (BS2)

Table 5.6.2 Data Transfer State (BS2)

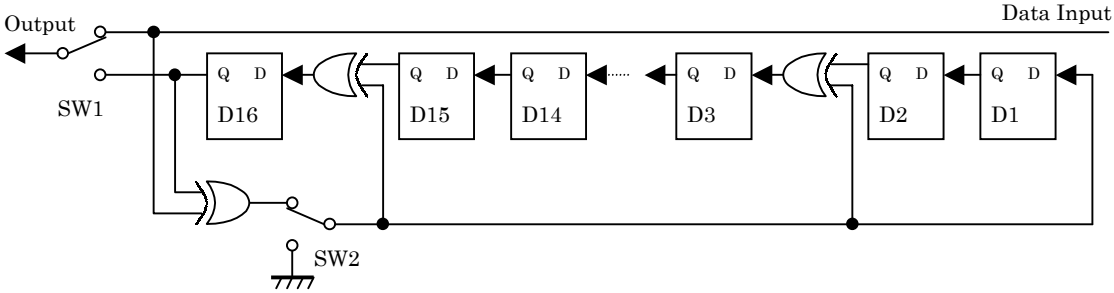
Host	In write packet, BS=Low is switched at timing ① and transfer is started from MSB of initial data at timing ③ which is 1 SCLK later. 16-bit CRC for all data are transferred just after the output of LSB of the final data. At timing ⑤, LSB of CRC is transmitted and BS=High is switched simultaneously, and the reception of BSY of BS3 (Handshake State) is started from timing ⑧.
Memory Stick	BS=Low is detected at timing ②, and reception is started from MSB of initial data at timing ④. At timing ⑥, LSB of CRC is received and BS=High is detected simulaneously, and BSY output of BS3 (Handshake State) is started from timing ⑦.

- If TPC errors arise in TPC state, Memory Stick shifts to BS0 in Two State Access Mode without receiving data.
- In case Data State is continued after CRC transferred, High should be output on SDIO during that period.
- CRC Specifications

  16-bit CRC, which is the remainder after transfer data is divided by G(X), is transferred by MSB First. Transfer timing is immediately after the data. (See Fig. 5.6.3)

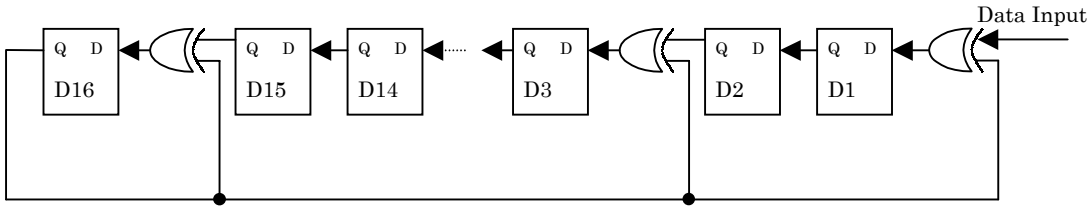
Formula : CRC16:G(X) = $X^{16} + X^{15} + X^2 + 1$

(1) CRC16 generating circuit (Output Data(n Byte)+CRC(16 Bit))



D1~16 initial value : All 0
Input data (bit string) : Output data (n Byte), MSB First
Switch status
SW1=Up & SW2=Up : CRC16 is being calculated (at data output)
SW1=Down & SW2=Down : at CRC16 output

(2) CRC16 check circuit (Input Data(n Byte)+CRC(16 Bit))



D1~16 initial value : All 0
Input data (bit string) : Input data(n Byte)+input CRC16(2 Byte), MSB First
Check result : Value for D16～1 are All 0 = No error
Other than above = bit error

Fig. 5.6.3 CRC16 Definition

5.6.3. Data Transfer State (BS3 : Read Packet)

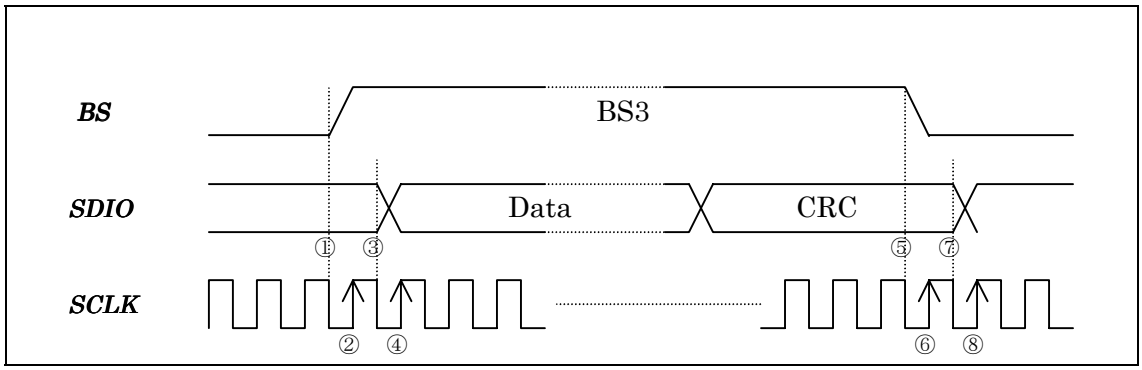


Fig. 5.6.4 Data Transfer State(BS3)

Table 5.6.3 Data Transfer State (BS3)

Host	In read packet, after switching to BS=High at timing ①, it starts receivingfrom MSB of initial data at timing ④. LSB of CRC is received at timing ⑥ after switching to BS=low at timing ⑤, and ends read packet.
Memory Stick	BS=High is detected at timing ②, and output is started from MSB of initial data from timing ③. After the output of LSB of CRC at timing ⑤, BS=Low is detected at timing ⑥ and shifts to BS0.

- In case Data State is continued still after CRC transfer, High should be output on SDIO during that period.
- Protocol terminates normally even if CRC error is detected on Host, however, retry process shall be executed on Host.

5.6.4. Handshake State (BS3 in Write Packet, BS2 in Read Packet)

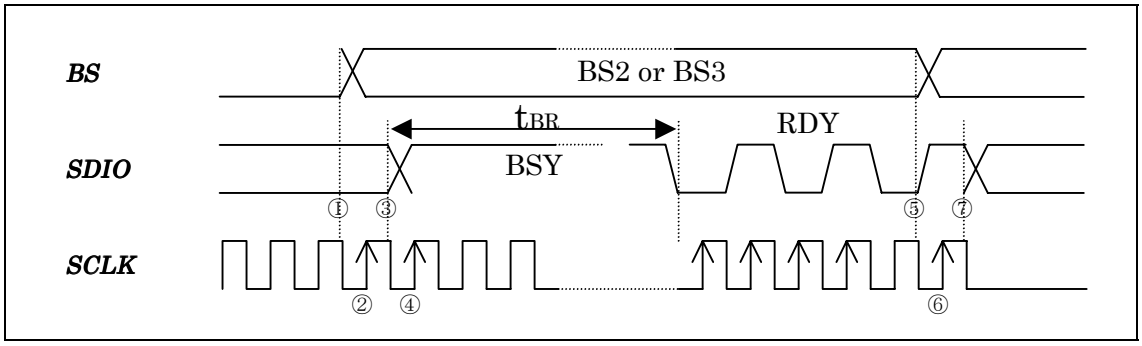


Fig. 5.6.5 Handshake State

Table 5.6.4 Handshake State

Host	BSY detection is started from timing ④ after switching BS at timing ①. After receiving more than 4 SCLK of RDY signal which inverts every 1 SCLK, and switching BS signal at timing ⑤, the succeeding state is started from timing ⑦.
Memory Stick	BSY signal output is started from timing ③ after switching BS is detected at timing ②. The next state is started from timing ⑦ after RDY signal is output by Memory Stick internal process termination and switching to BS is detected at timing ⑥.

- BSY Definition

  The state in which a signal on SDIO continues over 2 SCLK.

  In Four State Access Mode, SDIO becomes High.

  In Two State Access Mode, SDIO becomes Low by pull down because of high impedance.
- RDY Definition

  RDY is a state where SDIO toggles between Low and High every 1 SCLK.

  If Handshake State is terminated without RDY signal output for at least 4 SCLK on Memory Stick, Host determines that the RDY signal could not be received correctly, and cancels the operation by the TPC just before it.
- Memory Stick starts a cancel operation if Host switches BS(Bus State) before outputting RDY for 4 SCLK. Care must be taken because there may be a perception gap between Host and Memory Stick regarding operation status.
- The shortest length of BSY period is not prescribed.
- The longest length of RDY period is not prescribed.
- It is recommended to consider a time out after waiting more than 16 SCLK(t_{BR} max + RDY 4 SCLK).

♦ Memory Stick operation at Handshake state in read packet and write packet are shown below.

Table 5.6.5 BSY/RDY Specification

Packet	SDIO output	Description
Write Packet	BSY	In process of determining packet termination.
	RDY	Packet termination results have been reflected to the register.
Read Packet	BSY	In process of preparing transfer of the requested data.
	RDY	TPC is correct, and data transfer preparation is completed.
Error	No Output	Nothing is output because the Two State Access Mode is started.

♦ Definition of the RDY Timeout

Table 5.6.6 RDY Timeout Specification

Symbol	Item	Min.	Max.	Unit
t_{BR}	From BSY output to RDY output in normal operation.	−	12	SCLK
$t_{BR※}$	From BSY output to RDY output at wake time.	−	1	ms

※When Memory Stick receives a specific TPC while it is in sleep state, it wakes up and executes the TPC. In this case, BSY period is longer than that of normal state. If Host terminates Handshake State before receiving RDY output, Memory Stick enters into sleep state again.

5.6.5. INT Transfer State

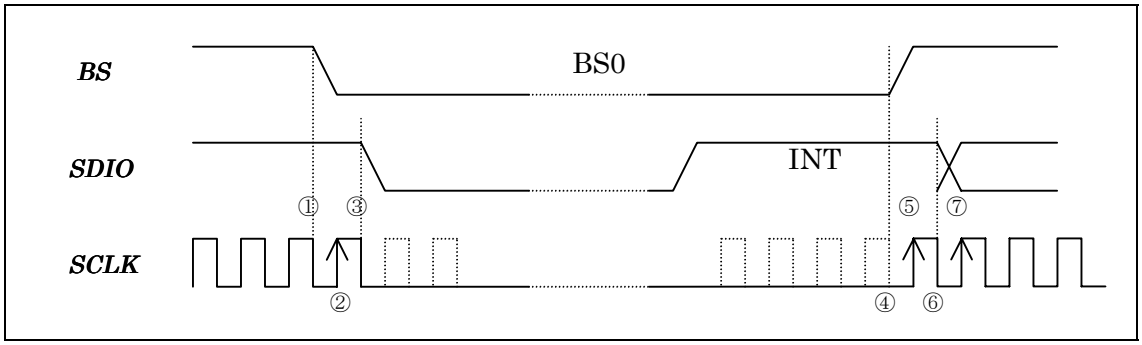


Fig. 5.6.6 INT Transfer State (BS0)

Table 5.6.7 INT Transfer State(BS0)

Memory Stick	BS0 is detected at timing ②, and INT Transfer Mode is started from timing ③. Interrupt occurrence factor is reflected to INT Register (described later), and SDIO=High is output during INT Transfer State period.
Host	SCLK output can be terminated after timing ③. (SCLK=Low). When SDIO=High is detected during the period of INT Transfer State, INT register of Memory Stick is read and the interrupt factor is checked.

- INT Definition

  A signal, outputs without synchronizing with SCLK.

  High Level : Interrupt signal is being output from Memory Stick.

  Low Level : There is no INT or INT has been validated.
- INT is output during BS0 period at Four State Access Mode operation (normal state).
- INT is not output during BS0 period at Two State Access Mode operation.
- INT output is cleared and SDIO is returned to Low when INT Register is read or RESET CMD is accepted.
- Since INT is not output under the following conditions, the signal level at BS0 is invalid:

  (1) When power supply is on.

  (2) When Memory Stick is at Two State Access Mode.

5.7. Transfer Protocol Command (TPC)

Host can access directly to Registers and PageBuffer on Memory Stick by TPC. TPC code is described below.

5.7.1. TPC Code

Table 5.7.1 TPC Code

D7	D6	D5	D4	D3	D2	D1	D0

Table 5.7.2 TPC Code Specification

Name	TPC 3	TPC 2	TPC 1	TPC 0	Operation
READ_PAGE_DATA					Transfer from PageBuffer
READ_REG					Read Register
GET_INT					Read INT Register
WRITE_PAGE_DATA					Transfer to PageBuffer
WRITE_REG					Write register
SET_R/W_REG_ADRS					Address setting of READ_REG WRITE_REG
SET_CMD					Set CMD
Reserved					
Disabled					

5.7.2. Description of TPC

Table 5.7.3 TPC Function Specification

TPC	Description
READ_PAGE_DATA	TPC for reading from PageBuffer in units of page (= 512 Bytes). Data is fixed-length of 512Byte+CRC16bit.
READ_REG	TPC for reading from the Register which address was set. Address and Data length are set by SET_R/W_REG_ADRS. (Actual Data length: the value which was set +CRC16bit)
WRITE_PAGE_DATA	TPC for writing to PageBuffer in units of page (= 512Bytes). Address and Data are fixed-length of 512Byte+CRC16bit.
WRITE_REG	TPC for writing to the Register which address was set. Address and Data length are set by SET_R/W_REG_ADRS. (Actual Data length: the value which was set +CRC16bit)
SET_R/W_REG_ADRS	TPC for setting values which determine the Register accessed by WRITE_REG and READ_REG. Values to be set are the following 4Bytes (fixed-length). Data is fixed-length of 4Bytes+CRC16bit. Starting address for READ_REG : Starting address of the Register to be read Consecutive size for READ_REG : The number of Registers to be read consecutively. Starting address for WRITE_REG : Starting address of the Register to be written Consecutive size for WRITE_REG : The number of Registers to be written consecutively.
SET_CMD	CMD to be executed by Flash Memory Controller, such as operation for Flash Memory is transferred. Data is fixed-length of CMD8bit+CRC16bit. Flash memory controller starts operation when CMD is set by this TPC, and posts the result by INT.
GET_INT	Only INT Register l Byte is read. Setting by SET_R/W_REG_ADRS TPC is not necessary. Read INT Register operation is provided as an independent TPC, as INT Register is accessed frequently. Data is fixed-length of 1Byte+CRC16bit.

5.7.3. List of Registers

The list of registers and buffers to be accessed by TPC are shown below.

5.7.3.1. Register Group Accessible by READ_REG/WRITE_REG

Registers which are accessible by READ_REG/WRITE_REG are shown below.

Table 5.7.4 Status Registers

	Register Name	R/W	Description of Contents
	Reserved	—	
	INT Register	R	Register of interruption factor
	StatusRegister0	R	Status of System
	StatusRegister1	R	CMD execution status
	Reserved	—	

Table 5.7.5 Parameter Registers

	System Parameter	W	System Parameter
	Block Address 2 ~ 0	W	The Block Address to access is designated.
	CMD Parameter	W	Command Parameter
	Page Address	W	The Page Address to access is designated.
	Page Address	R	Accessed Page Address

Table 5.7.6 ExtraDataRegisters (Write Only)

	OverwriteFlag	W	Management Flag Register which can be overwritten.
	ManagementFlag	W	Management Flag Register
	Logical Address 1 ~ 0	W	Logical Address
	Reserved Area 4 ~ 0	W	Reserved Area

Table 5.7.7 ExtraDataRegisters (Read Only)

	OverwriteFlag	R	Overwrite Management Flag
	ManagementFlag	R	Management Flag
	Logical Address 1 ~ 0	R	Logical Address
	Reserved Area 4 ~ 0	R	Reserved Area

Note) Specifications on extra data register conform to the format definition. (See Section 7 Physical Format.)

5.7.3.2. Register Group Not Accessible by READ_REG, WRITE_REG TPC

Registers accessible only by specific TPC are shown below.

5.7.3.2.1. Registers Accessed by SET_R/W_REG_ADRS TPC

Table 5.7.8 R/W REG TPC ADRS Registers

—	READ_ADRS	W	The starting address read by READ_REG
—	READ_SIZE	W	The number of bytes read by READ_REG
—	WRITE_ADRS	W	The starting address written by WRITE_REG
—	WRITE_SIZE	W	The number of bytes written by WRITE REG

5.7.3.2.2. Registers Accessed by SET_CMD TPC

Table 5.7.9 CMD Register

—	CMD_REG	W	Sets CMD to be executed.

5.7.3.2.3. Page Buffer

The internal buffer for data read/write of Flash Memory which is accessed by READ_PAGE_DATA, WRITE_PAGE_DATA TPC. The size is 512Bytes, the same as the page size of Flash Memory.

Table 5.7.10 Page Buffer

—	PAGE_BUFFER	R/W	Buffer for Flash Memory data area

5.8. Registers

Registers of Memory Stick are classified into the following four according to their functions:

- Status Registers : Registers to show the internal status of Memory Stick.
- Parameter Registers : Registers to set parameter for Memory Stick command operation.
- ExtraDataRegisters : Registers to Read/Write management information in ExtraDataArea.
- Other Registers : Registers accessed by other than READ_REG/WRITE_REG TPC.

Each register is explained as below: (The values in upper row for each bit are the default values.)

5.8.1. Status Register

Status Register is a group of registers to show the operation status of Flash Memory Controller in Memory Stick, the PageBuffer status and the operation results of SET_CMD TPC.

5.8.1.1. INT Register

Table 5.8.1 INT Register Default

	D7	D6	D5	D4	D3	D2	D1	D0
INT Register	0 CED	0 ERR	0 BREQ	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 CMDNK

Table 5.8.2 INT Register Specification

CED	ERR	BREQ	CMDNK	Operation status
1	0	X	0	Normal termination
1	1	X	0	CMD error termination
X	0	1	0	Data request (BLK_READ BLK_WRITE) under normal conditions.
X	1	1	0	Data request (BLK_READ)at error occurrence
0	X	0	0	During CMD execution, ERR bit becomes ineffective.
X	X	X	1	CMD not acceptable

A Register, informs the status of Memory Stick operation to Host. When the Flash Memory Controller on Memory Stick operates by SET_CMD TPC, 1 is set in each bit of INT Register, and INT is generated at INT Transfer State(BS0) in Serial I/F.
See Section 6 for details for generation timing etc.

- CED (Command EnD)
  CED indicates the end of CMD executed by SET_CMD TPC.
  It is reset at initial status and CMD start time, and set at CMD termination.
- ERR (ERRor)
  ERR (ERRor) is a flag to indicate that a FlashError (Read, Write, Erase) has occured, by execution of BLOCK_READ, BLOCK_WRITE and BLOCK_ERASE CMD of SET_CMD TPC.
  It is reset at initial status and CMD start time, and set simultaneously with CED or BREQ. (At BREQ being set, it is reset simultaneously with BREQ Reset.)
  Details of Flash Read Error are shown in StatusRegister1.
- BREQ (Buffer REQuest)
  BREQ (Buffer REQuest) indicates the request to Host for access (READ_PAGE_DATA, WRITE_PAGE_DATA TPC) of PageBuffer by BLOCK_READ/BLOCK_WRITE CMD of SET_CMD TPC.
  At BLOCK_READ CMD execution, BREQ indicates request for PageBuffer read (BF=1) from Memory Stick to Host, and is reset by READ_PAGE_DATA TPC.
  At BLOCK_WRITE CMD execution, BREQ indicates request for PageBuffer write (BE=1) from Memory Stick to Host, and is reset by WRITE_PAGE_DATA TPC.
- CMDNK(CoMmanD NacK)
  Indicates that the CMD which is set by SET_CMD TPC from Host cannot be executed. It is set when non-executable CMD is received, and reset when executable CMD is received. When CMDNK bit is 1, other bits of INT Register are of indefinite value.

5.8.1.2. Status Register0

Table 5.8.3 Status Register0 Default

	D7	D6	D5	D4	D3	D2	D1	D0
StatusRegister0	0 MB	0 FB0	1 BE	0 BF	0 Reserved	0 Reserved	0 SL	X WP

Status Register0 shows Flash Memory Controller operation status and PageBuffer status.

- MB(Media Busy)
  Indicates that CMD transferred by SET_CMD TPC is in execution.
- FB0 (Flash Busy 0)
  Indicates that Flash Memory Chip is operating by flash control command transferred by SET_CMD TPC.
  (FB=1 when MB=0, indicates a malfunction status. See Section 6.2.10 for how to recover from it.)
- BE (Buffer Empty)
  Indicates that PageBuffer of Memory Stick is empty.
  It changes by access from Host or access by Flash Memory Controller.
- BF (Buffer Full)
  Indicates that data exists in PageBuffer of Memory Stick.
  It changes by the access from Host or the access by Flash Memory Controller.
- SL (SLeep)
  Memory Stick is in sleep status (internal clock oscillation stop).
  1 on the completion of sleep action
  0 on the completion of wake action
- WP (Write-Protect)
  Indicates Write-Protect switch state. ON : 1 / OFF : 0

5.8.1.3. StatusRegister1

Table 5.8.4 Status Register1 Default

	D7	D6	D5	D4	D3	D2	D1	D0
Status Register1	0 MB	0 FB1	0 DTER	0 UCDT	0 EXER	0 UCEX	0 FGER	0 UCFG

A register to indicate the operating status of Flash Memory Controller, the location of FlashReadError and whether it can be corrected or not.

- MB(Media Busy)
  The same as MB in Status Register 0.
- FB 1(Flash Busy 1)
  During Flash Memory Chip is operating at MB=1, FB1 is set at 1.
  Even if FB0=1 of Status Register 0 at MB=0, FB1 shall be set at 0 as it is masked by MB.
- DTER(DaTa ERror)
  Error (Write Error, Erase Error, Read Data Area ECC Error) in DataArea.
- UCDT (Unable to Correct DaTa)
  Data cannot be corrected in DataArea when DTER is 1 at BLOCK_READ.
- EXER (EXtra data ERror)
  ECC Error of data in NonOverWriteArea of ExtraDataArea excluding Overwite Flag, at BLOCK_READ.
- UCEX (Unable to Correct EXtra data)
  Data in NonOverwriteArea of ExtraDataArea cannot be corrected at BLOCK_READ.
- FGER (FlaG ERror)
  Bit error occurred in OverwriteFlag of ExtraDataArea at BLOCK_READ.
- UCFG (Unable to Correct FlaG)
  OverwriteFlag of ExtraDataArea cannot be corrected at BLOCK_READ.

5.8.2. Description of Parameter Register

5.8.2.1. System Parameter

Table 5.8.5 System Parameter Default

	D7	D6	D5	D4	D3	D2	D1	D0
System Parameter	1 BAMD	0 ATEN	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 —

It is the mode parameter of the entire operation of Memory Stick. Normally, the above default values are used.

- BAMD (Block Address MoDe)
  Mode of Block Address to execute BLOCK_READ, BLOCK_WRITE and BLOCK_ERASE CMD.
  0 : Chip Mode : 1Byte of Block Address 2 is used as chip address. (Disabled)
  1 : Linear Mode : Can be used as contiguous area.
- ATEN (ATtribute rom ENable)
  READ_PAGE_DATA TPC accesses to AttributeROM, not to page buffer, when the state is Enable.
  0 : Disable
  1 : Enable (Disabled except at Boot Block creation. See Section 7, Physical Format.)

5.8.2.2. Command Parameter

Table 5.8.6 Command Parameter Default

	D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter	0 CP2	0 CP1	0 CP0	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved

Table 5.8.7 Command Parameter Specification

CP2	CP1	CP0	Operation Mode
0	0	0	Block Access of Data Area + Extra Data Area Access till the final page with Page Address value as initial value.
0	0	1	1-page access of Data Area + Extra Data Area
0	1	X	1-page access of Extra Data Area only
1	X	X	Overwrite of Overwrite Flag in Extra Data Area. 1-page access (BLOCK_WRITE CMD only)

The area of data to be accessed is designated when BLOCK_READ/BLOCK_WRITE CMD of SET_CMD, TPC is executed.

(1) Block Access Mode (DataArea + ExtraDataArea)
Access starts from the page shown in Page Address Register and continues page by page until the final page or the end by BLOCK_END.
DataArea value is accessed through PageBuffer and ExtraDataArea value is accessed through ExtraDataRegister.

(2) Single Page Access Mode (DataArea + ExtraDataArea)
Accesses to the page shown in Page Address Register.
DataArea value is accessed through PageBuffer and ExtraDataArea value is accessed through ExtraDataRegister. Ends in 1-page operation.

(3) Extra Data Access Mode (1-page access in ExtraDataArea only) : Write
ExtraDataRegister setting value is written in ExtraDataArea.
Ends in 1-page operation.

(4) Extra Data Access Mode (1-page access in ExtraDataArea only) : Read
The value is written in ExtraDataRegister by reading only the Data in ExtraDataArea.
Ends in 1-page operation.

(5) Overwrite Access Mode (Write the OverwriteFlag in ExtraDataArea)
Overwrites the OverwriteFlag value of ExtraDataRegisters which was previously written.
Therefore, the value of the data to be written becomes masked.
Ends in 1-page operation.

5.8.2.3. Block Address 2~0 (Write Only)

Table 5.8.8 Block Address 2~0 Default

	D7	D6	D5	D4	D3	D2	D1	D0
BlockAddress2	0 BA23	0 BA22	0 BA21	0 BA20	0 BA19	0 BA18	0 BA17	0 BA16
BlockAddress1	0 BA15	0 BA14	0 BA13	0 BA12	0 BA11	0 BA10	0 BA9	0 BA8
BlockAddress0	0 BA7	0 BA6	0 BA5	0 BA4	0 BA3	0 BA2	0 BA1	0 BA0

Effective when BLOCK_READ, BLOCK_WRITE or BLOCK_ERASE CMD of SET_CMD TPC is executed. Effective BlockAddress is obtained from the Boot Block information (see Section 7 Physical Format). When invalid BlockAddress is set, INT by CMDNK is generated by issuing SET_CMD TPC.

5.8.2.4. Page Address (Write Only)

Table 5.8.9 Page Address Default

	D7	D6	D5	D4	D3	D2	D1	D0
Page Address	0 PA7	0 PA6	0 PA5	0 PA4	0 PA3	0 PA2	0 PA1	0 PA0

Effective when BLOCK_READ or BLOCK_WRITE CMD of SET_CMD TPC is executed.

Effective PageAddress of physical PageAddress in a Block is obtained from the Boot Block information (See Section 7 Physical Format).

When invalid PageAddress is set, INT by CMDNK is generated by issuing SET_CMD TPC.

5.8.2.5. Page Address (Read Only)

Table 5.8.10 Page Address Default

	D7	D6	D5	D4	D3	D2	D1	D0
Page Address	0 PA7	0 PA6	0 PA5	0 PA4	0 PA3	0 PA2	0 PA1	0 PA0

Page Address that is still under operation or operation finished (including Error), when BLOCK_READ or BLOCK_WRITE CMD of SET_CMD TPC is being executed. In Block Access Mode, value is incremented when the operation of the next page starts.

- BLOCK_WRITE : Incremented at the timing when starts transferring of new page data from PageBuffer in BF=1 state of Status Register0 to Flash Memory.
- BLOCK_READ : Incremented at the timing when starts transferring of new data from Flash Memory on Memory Stick to PageBuffer in BE=1 state of StatusRegister0.

5.8.3. Extra Data Registers (Write Only)

A Register (write only register) for file management information etc. which will be written in ExtraDataArea of the same page together with the data on PageBuffer by BLOCK_WRITE CMD of SET_CMD TPC. It consists of two areas, one is to allow overwrite and the other is to prohibit overwrite.

See Section 7 for the definition of respective bits.

5.8.3.1. OverwriteArea

In this area, a register allowing overwrite is contained (OverwriteFlag).

Table 5.8.11 OverwriteFlag Default

	D7	D6	D5	D4	D3	D2	D1	D0
OverwriteFlag	1 BKST	1 PGST0	1 PGST1	1 UDST	1 Reserved	0 —	0 —	0 —

It is used as a flag to show the physical state of block or page, or information on logical/physical conversion table.

- BKST (BlocK Status) : Identifies the defective blocks which occur later.
- PGS0,1 (PaGe Status) : Shows the uncorrectable error which occurs at Reading.
- UDST (Update State) : Identifies the data usage state in block.
- At the time of erasure, bits D7 to D3 are High.
- In Overwrite Access Mode, each bit is independent and allows overwrite from 1 to 0.
- To overwrite after BLOCK_WRITE, the bit written in Low has to be masked by setting High (to avoid Flash Memory trouble).
- Each Bit has correcting ability, which is equal to or better than that of DataArea.

5.8.3.2. NonOverwrite Area

- Overwrite is not allowed. See Section 7 for the definition of respective bits.

5.8.3.2.1. ManagementFlag

Table 5.8.12 ManagementFlag Default

	D7	D6	D5	D4	D3	D2	D1	D0
ManagementFlag	1 Reserved	1 Reserved	1 SCMS0	1 SCMS1	1 ATFLG	1 SYSFLG	1 Reserved	1 Reserved

- SCMS: Bit for serial copy management
- ATFLG : Logical/physical conversion table identification flag
- SYSFLG : System flag

5.8.3.2.2. Logical Address 1 ~ 0

Table 5.8.13 Logical Address 1 ~ 0 Default

	D7	D6	D5	D4	D3	D2	D1	D0
LogicalAdr1	1 LADR15	1 LADR14	1 LADR13	1 LADR12	1 LADR11	1 LADR10	1 LADR9	1 LADR8
LogicalAdr0	1 LADR7	1 LADR6	1 LADR5	1 LADR4	1 LADR3	1 LADR2	1 LADR1	1 LADR0

5.8.3.2.3. Reserved Area 4 ~ 0

Table 5.8.14 Reserved Area 4 ~ 0 Default

	D7	D6	D5	D4	D3	D2	D1	D0
ReservedArea4	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved
ReservedArea3	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved
ReservedArea2	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved
ReservedArea1	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved
ReservedArea0	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved	1 Reserved

5.8.4. Extra Data Register (Read Only)

Management information written in ExtraDataArea on the same page, together with data on PageBuffer is read out at the under-mentioned register by BLOCK_READ CMD of SET_CMD TPC (Read only). See Section 7 for the definition of respective bits.

5.8.4.1. Overwrite Area

Table 5.8.15 OverwriteFlag Default

	D7	D6	D5	D4	D3	D2	D1	D0
OverwriteFlag	0 BKST	0 PGST0	0 PGST1	0 UDST	0 Reserved	0 —	0 —	0 —

Used as a flag to show the physical state of block or page, or information on logical/physical conversion table etc.

- When read error occurs, correction is executed at every bit independently.
- The error result is reflected on D1-0 of StatusRegister 1.
- Reading from normally erased Page is all High at D7-3 (BKST ~ Reserved).

5.8.4.2. NonOverwriteArea

The error result is reflected on D3-2 of StatusRegister 1.

Reading from normally erased page is all 0xFF. See Section 7 for detail.

5.8.4.2.1. ManagementFlag

Table 5.8.16 ManagementFlag Default

	D7	D6	D5	D4	D3	D2	D1	D0
ManagementFlag	0 Reserved	0 Reserved	0 SCMS0	0 SCMS1	0 ATFLG	0 SYSFLG	0 Reserved	0 Reserved

5.8.4.2.2. Logical Address 1 ~ 0

Table 5.8.17 LogicalAddress 1 ~ 0 Default

	D7	D6	D5	D4	D3	D2	D1	D0
LogicalAdr1	0 LADR15	0 LADR14	0 LADR13	0 LADR12	0 LADR11	0 LADR10	0 LADR9	0 LADR8
LogicalAdr0	0 LADR7	0 LADR6	0 LADR5	0 LADR4	0 LADR3	0 LADR2	0 LADR1	0 LADR0

5.8.4.2.3. ReservedArea 4 ~ 0

Table 5.8.18 ReservedArea 4 ~0 Default

	D7	D6	D5	D4	D3	D2	D1	D0
ReservedArea4	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved
ReservedArea3	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved
ReservedArea2	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved
ReservedArea1	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved
ReservedArea0	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved	0 Reserved

5.8.5. R/W REG TPC ADRS Registers

A Register sets the starting address and data length of READ_REG, WRITE_REG TPC. It is set only by SET_R/W_REG_ADRS TPC. Default values are also usable.

Table 5.8.19 R/W REG TPC ADRS Registers Default

Name	D7	D6	D5	D4	D3	D2	D1	D0
READ_ADRS	0 RA7	0 RA6	0 RA5	0 RA4	0 RA3	0 RA2	0 RA1	0 RA0
READ_SIZE	0 RS7	0 RS6	0 RS5	1 RS4	1 RS3	1 RS2	1 RS1	1 RS0
WRITE_ADRS	0 WA7	0 WA6	0 WA5	1 WA4	0 WA3	0 WA2	0 WA1	0 WA0
WRITE_SIZE	0 WS7	0 WS6	0 WS5	0 WS4	1 WS3	1 WS2	1 WS1	1 WS0

- READ_ADRS
  The starting address of the register which is read by READ_REG TPC.
- READ_SIZE
  Size from the starting address of the register which is read by READ_REG TPC.
  When the size is 0, it is handled as 256 bytes. (Transfer size = 1 ~256)
- WRITE_ADRS
  The starting address of the register which is written by WRITE_REG TPC.
- WRITE_SIZE
  Size from the starting address of the register which is written by WRITE_REG TPC.
  When the size is 0, it is handled as 256 bytes. (Transfer size = 1~256)

* Data transfer to RegisterAddress which is not specified, is invalid.

* Data read from RegisterAddress which is not specified, is undefined.

5.8.6. CMD Register

A register sets a operation command to Flash Memory Controller. It is accessible only by SET_CMD TPC. See Section 6 for each command in detail.

Table 5.8.20 CMD Register

Name	D7	D6	D5	D4	D3	D2	D1	D0
CMD Register	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

5.9. Acceptable TPC

StatusRegister0, shows the operating state of entire Memory Stick. TPC operation is restricted according to the state. It is recommended not to use TPC at status except those in list shown below.

Table 5.9.1 Acceptable TPC

StatusRegister0 / TPC	D7	D6	D5	D4	D1	D0
	MB	FB0	BE	BF	SL	WP
READ_PAGE_DATA	**0**	X	X	**1**	**0**	X
WRITE_PAGE_DATA	**0**	X	**1**	X	**0**	X
READ_PAGE_DATA	**1** *1	X	X	**1**	**0**	X
WRITE_PAGE_DATA	**1** *1	X	**1**	X	**0**	X
WRITE_REG	**0**	X	X	X	X	X
READ_REG	X	X	X	X	X	X
SET_R/W_REG_ADRS	X	X	X	X	X	X
SET_CMD	X	X	X	X	X	X
GET_INT	X	X	X	X	X	X

X : Don't care

- (Note)*1 Only MB = 1 by BLOCK_READ, BLOCK_WRITE CMD of SET_CMD TPC in DataArea access mode.
- It is not guaranteed when TPC is used in disabled state.
- Memory Stick does not generate RDY at Handshake State, and shifts to Two State Access Mode operation, when it receives unacceptable TPC.